

# 8SQ800 Schematics

Revision 1.0

SHEET	TITLE
1	COVER SHEET
2	BOM & PCB MODIFY HISTORY
3	BLOCK DIAGRAM
4,5,6	INTEL CPU_WMT_478
7-11	SIS655 (NORTH BRIDGE) HOST; DDR; AGP,HYPER ZIP
12-15	SIS963 (SOUTH BIRDGE)
16	CLOCK GENERATOR (CY28381)
17	DDR CLOCK BUFFER
18,19	DDR SDRAM DIMMS 1,2,3,4
20	DDR TERMINATION
21	AGP 8X SLOT
22,23	PCI SLOT 1,2,3,4,5
24	IDE,FRONT USB,PCIRST#
25	LPCIO_IT8705
26	DUAL BIOS
27	COM, LPT, FDD, KB/MS, IR
28	AC 97 ALC650
29	AUDIO JACK,GAME PORT
30	FAN, SMB PORT
31	PANEL,STR LED,FANS ,CI
32	VCORE 3-PHASE PWM HIP 6302 + 6602+6601
33	VDDQ,VCC18,VCCVID DC POWER

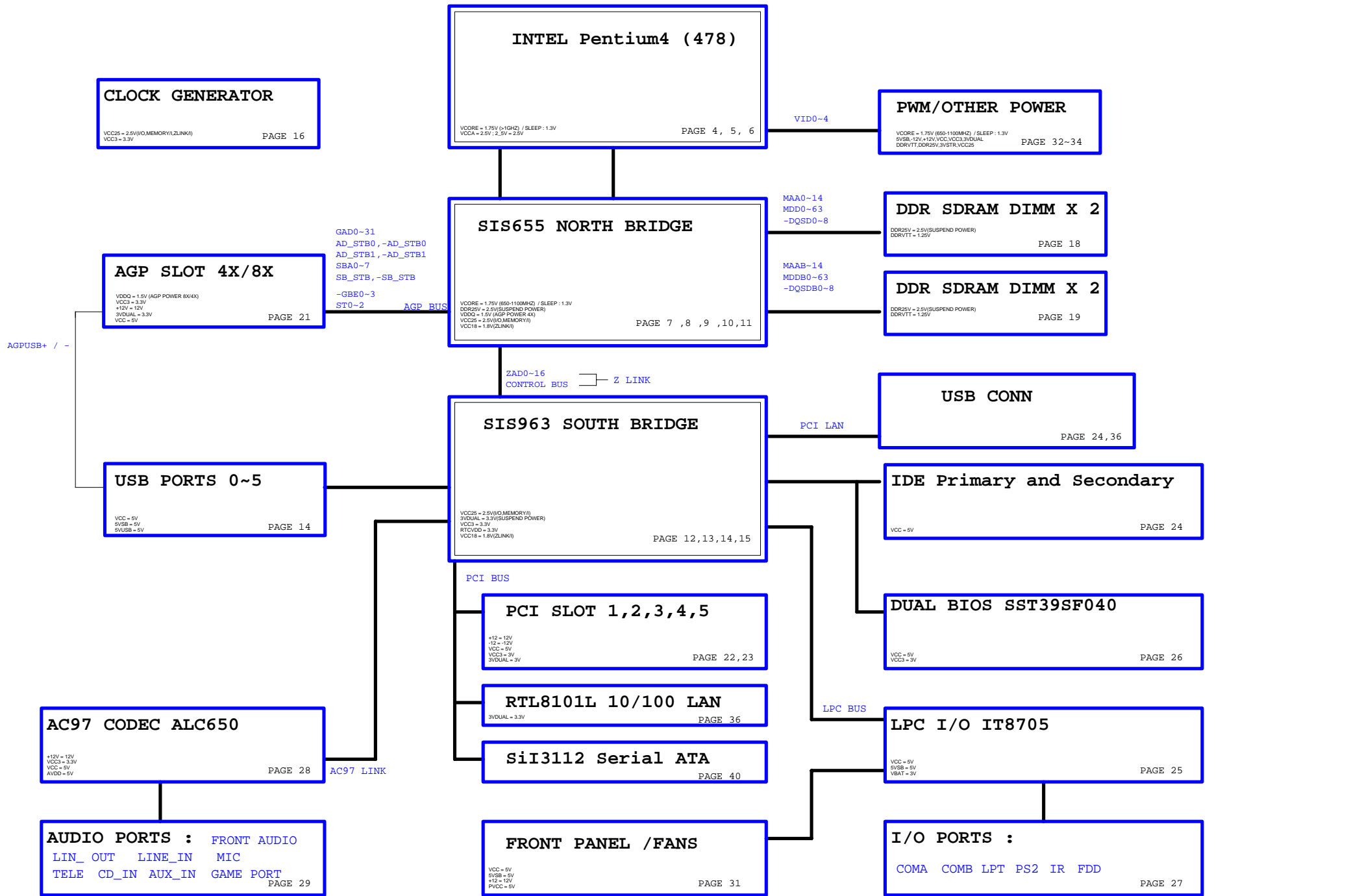
SHEET	TITLE
34	DDR POWER
35	ATX CONN, GPIO LIST
36	RTL8101L
37, 38	IT8212 IDE RAID
39	ASIC1 & AT123(PCI ARBITOR)
40	SiI3112 Serial ATA

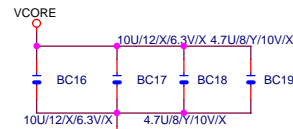
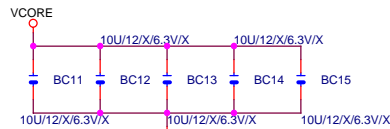
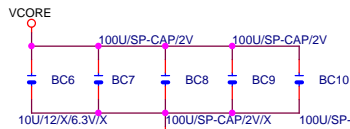
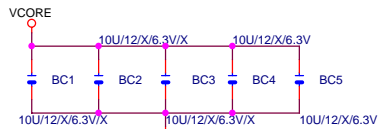
PCB Size: 305\*244 mm

<b>GIGABYTE</b>		
<b>COVER SHEET</b>		
Title		
Size	Document Number	Rev
Custom	<b>GA-8SQ800</b>	<b>1.0</b>
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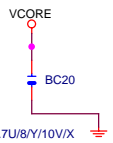
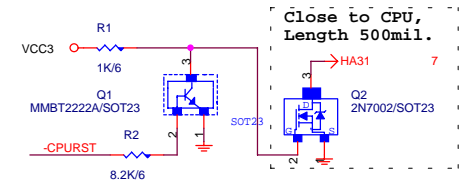


# 8SQ800 BLOCK DIAGRAM





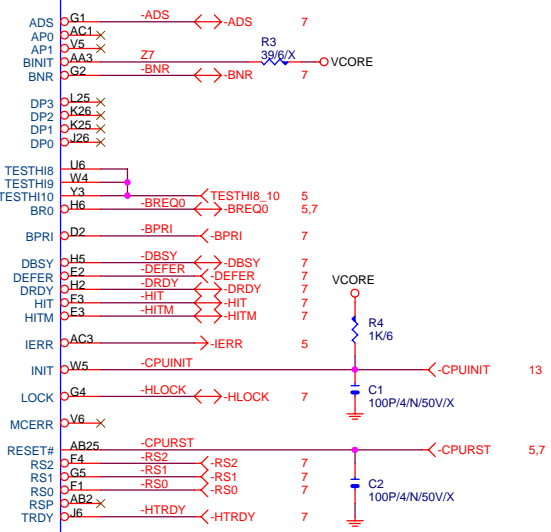
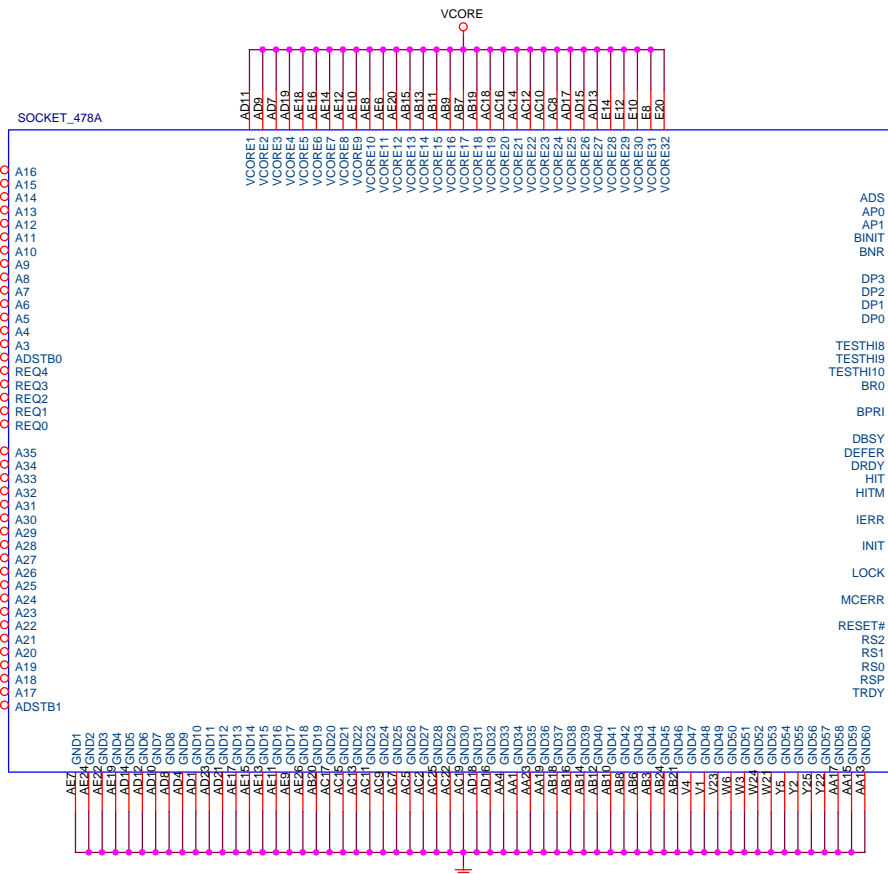
For Hyper Threading CPU disable circuit.



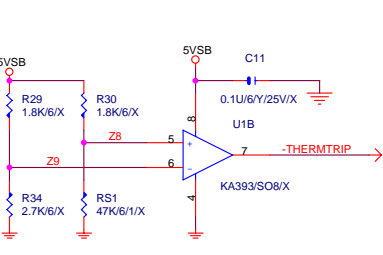
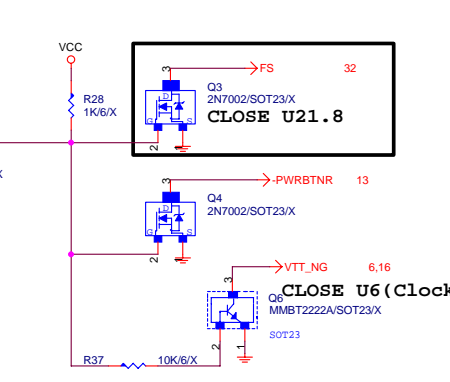
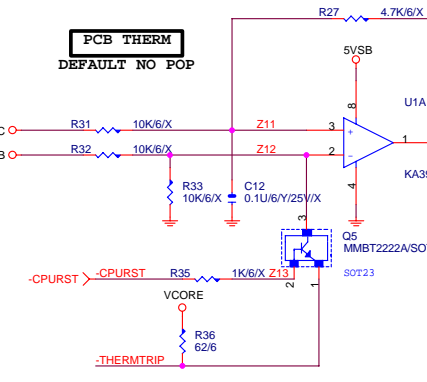
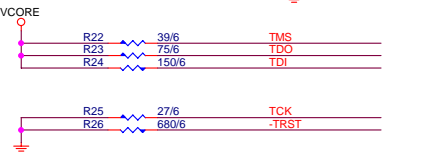
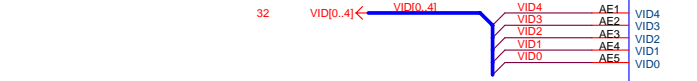
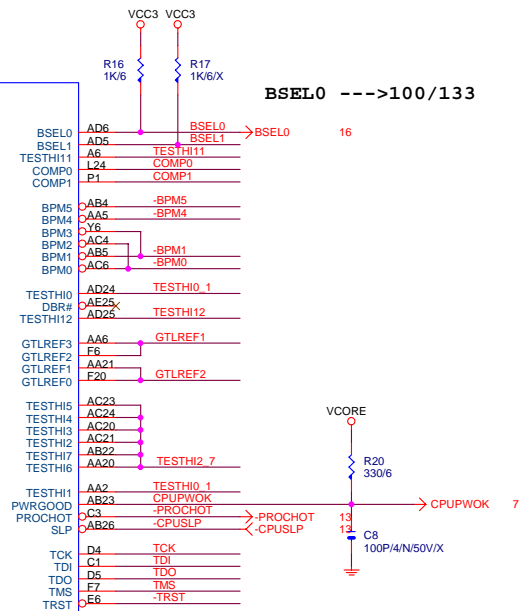
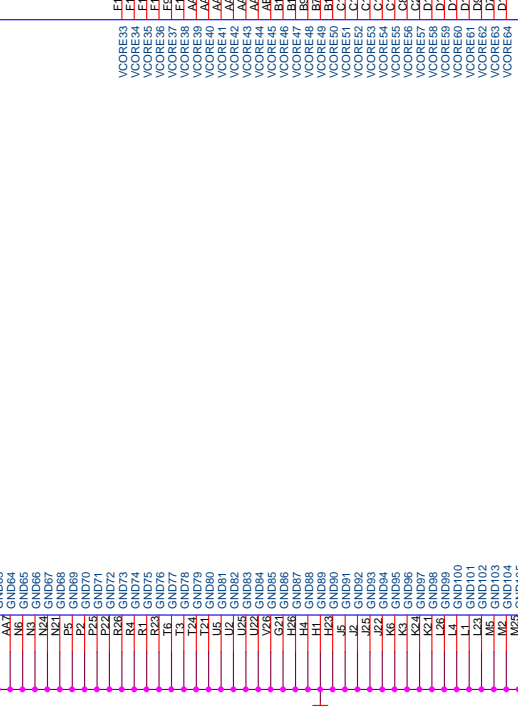
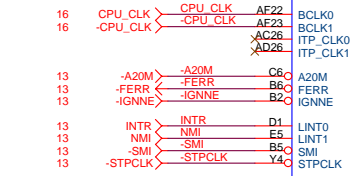
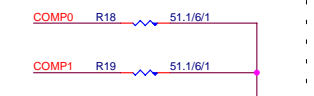
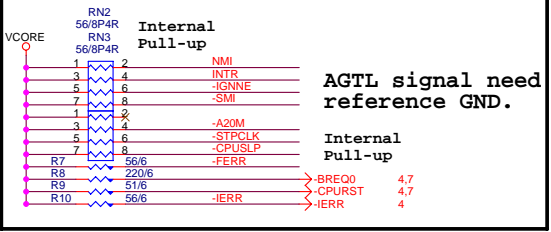
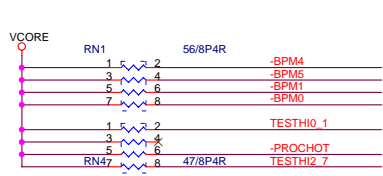
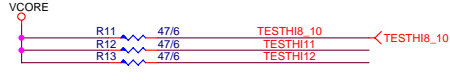
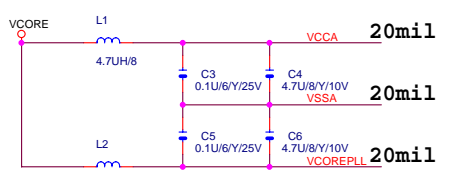
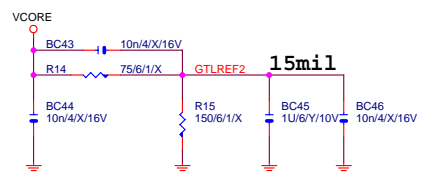
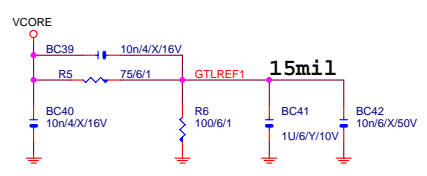
上2顆SP-CAP 100uF,  
2顆10U/X5R電容

Socket內放3顆SP-CAP  
與6顆1206共LAYOUT

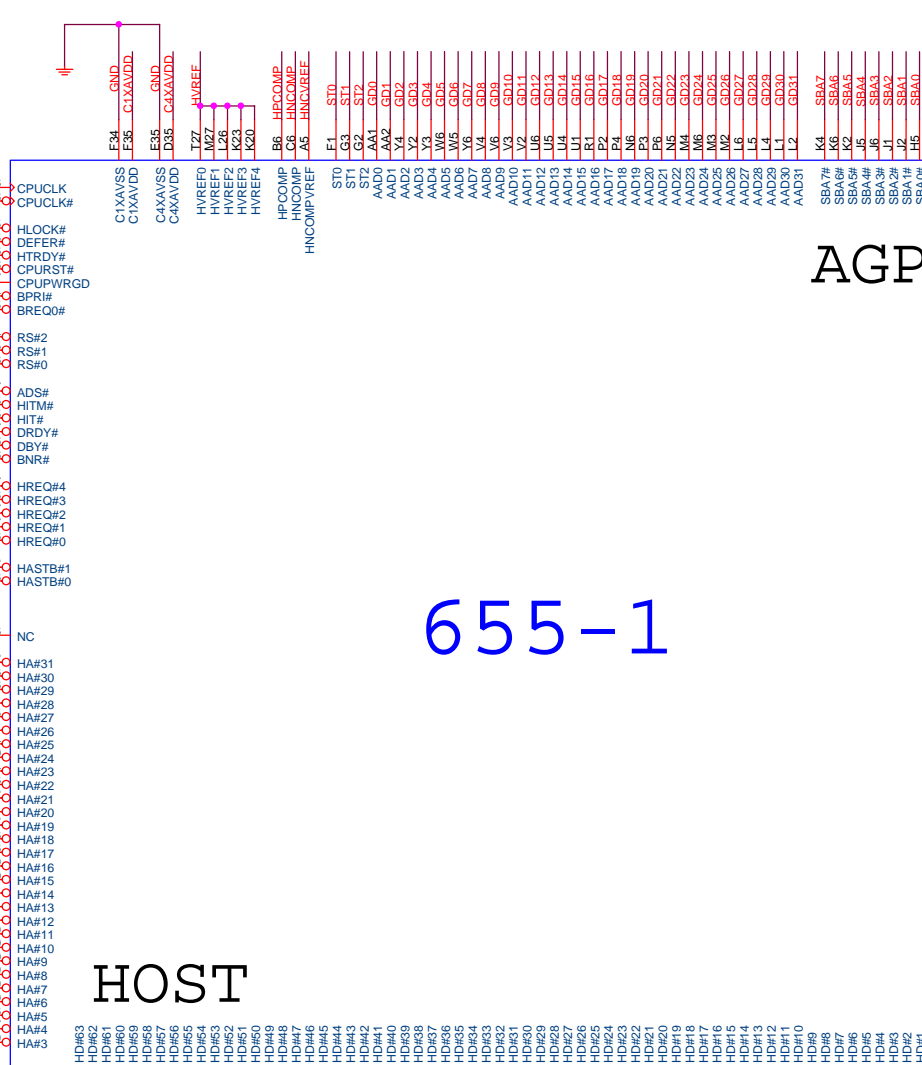
Socket外放1顆SP-CAP  
與2顆1206共LAYOUT



<b>GIAGBYTE</b>			
Title			
<b>WILLAMETTE 1/3</b>			
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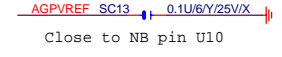
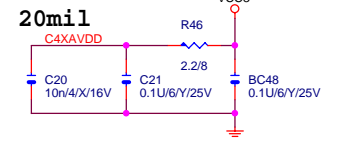
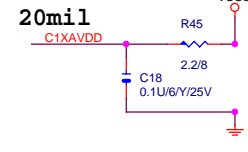
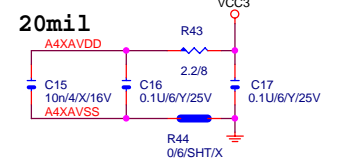
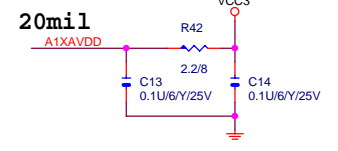
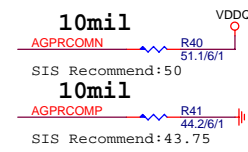
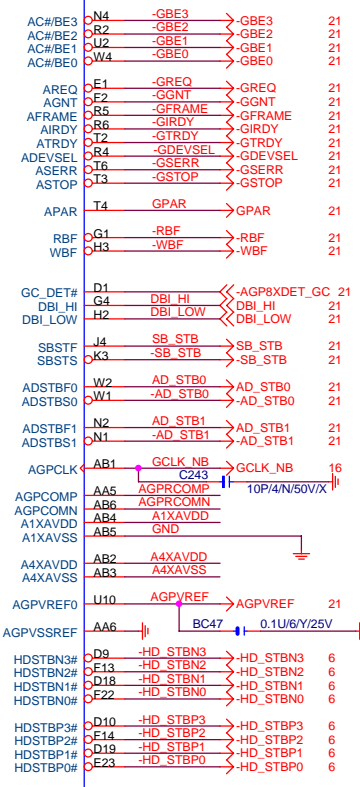




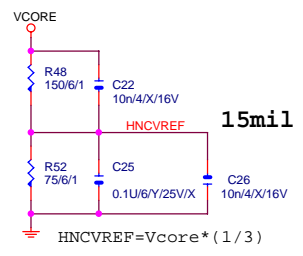
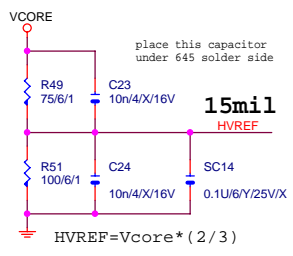
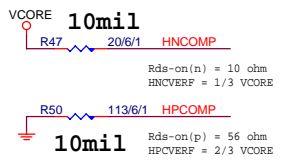
AGP

HOST

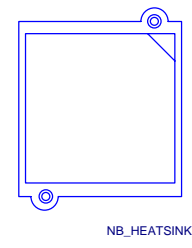
655-1



Close to NB pin U10



N.B HEATSINK

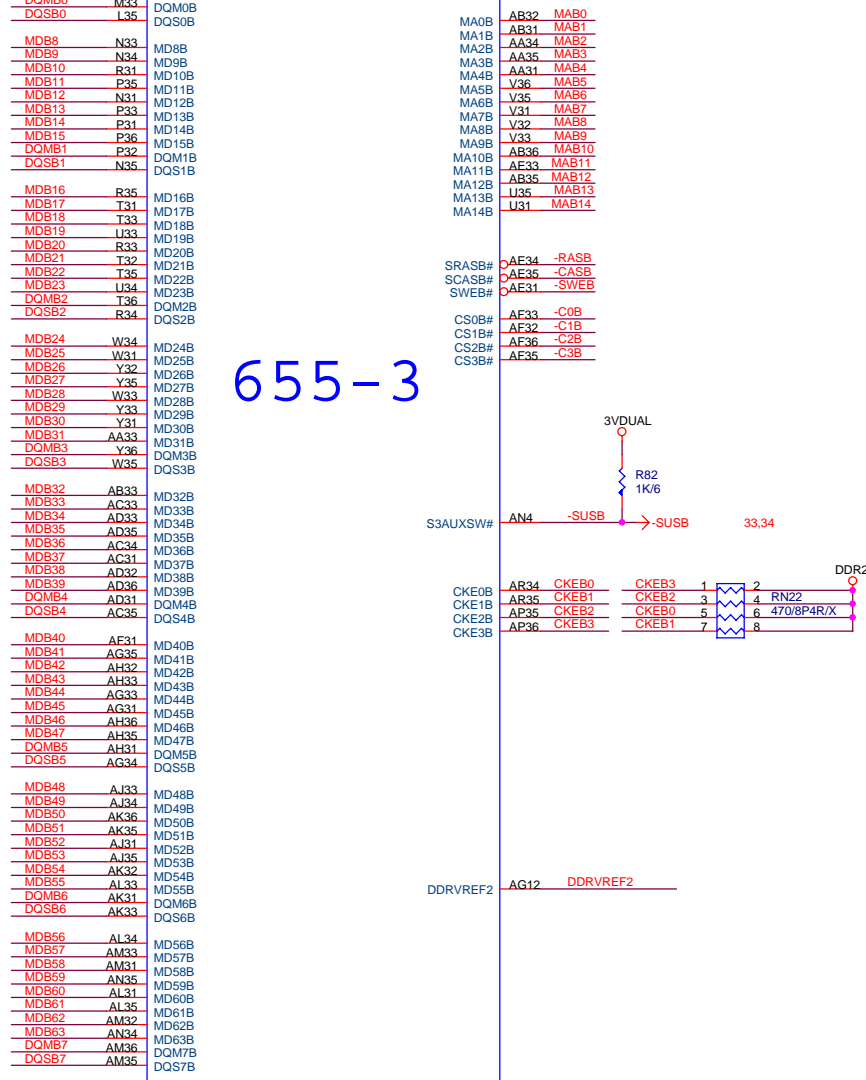
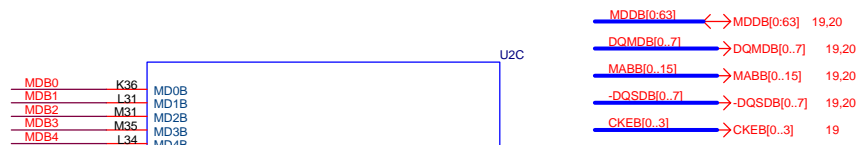


<b>GIGABYTE</b>		
<b>SIS655-1(HOST/AGP)</b>		
Title	Document Number	Rev
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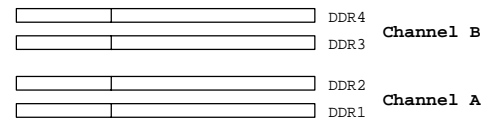
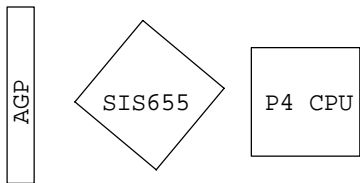
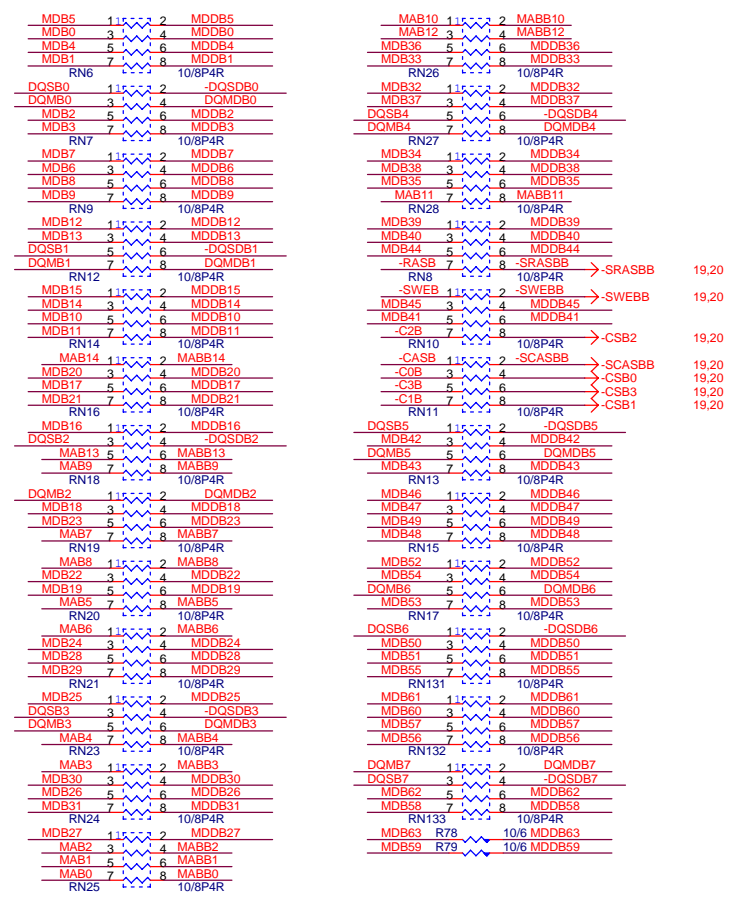
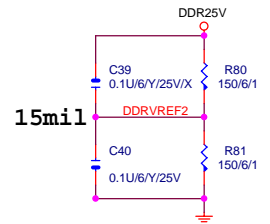
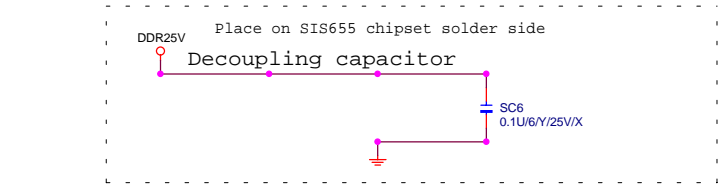




# DDR DAMPING Near DIMM4



655-3



Channel A: Solder Side.  
Channel B: Component Side.

**GIGABYTE**

**SIS655-3(DDR-B)**

Title

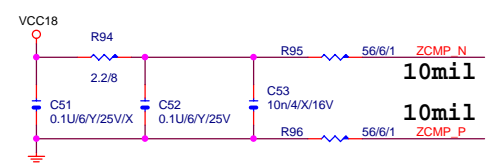
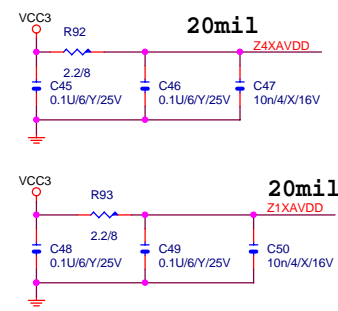
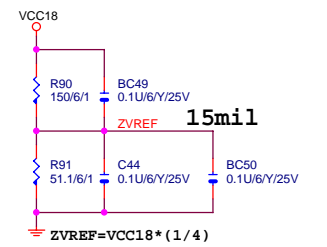
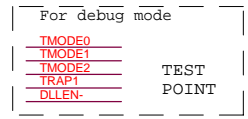
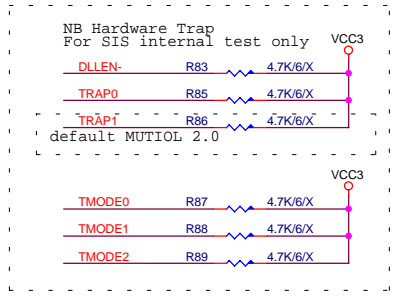
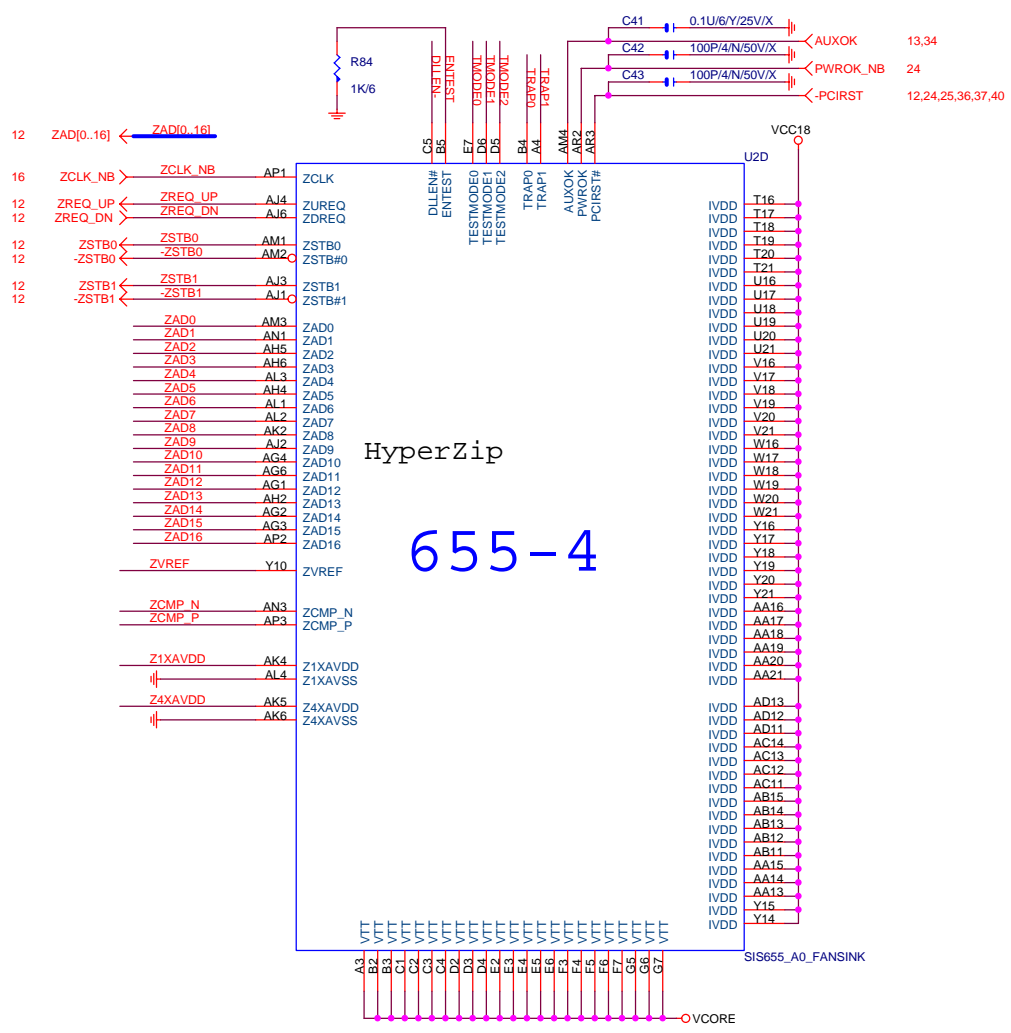
Size Custom Document Number

GA-8SQ800

Date: Thursday, December 26, 2002

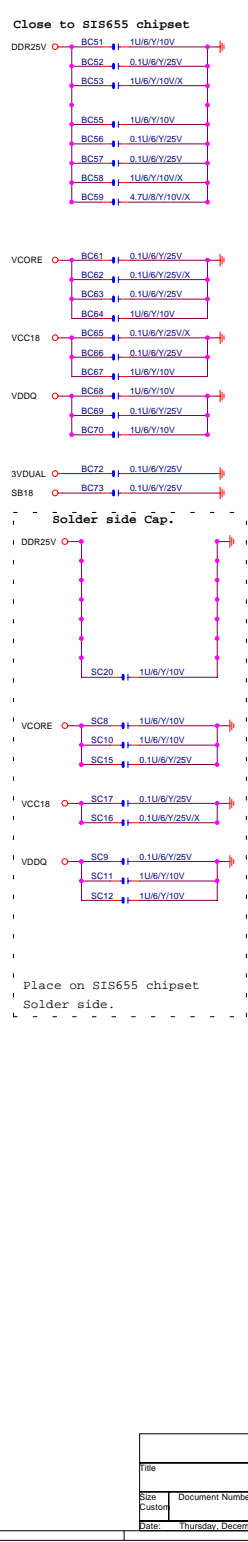
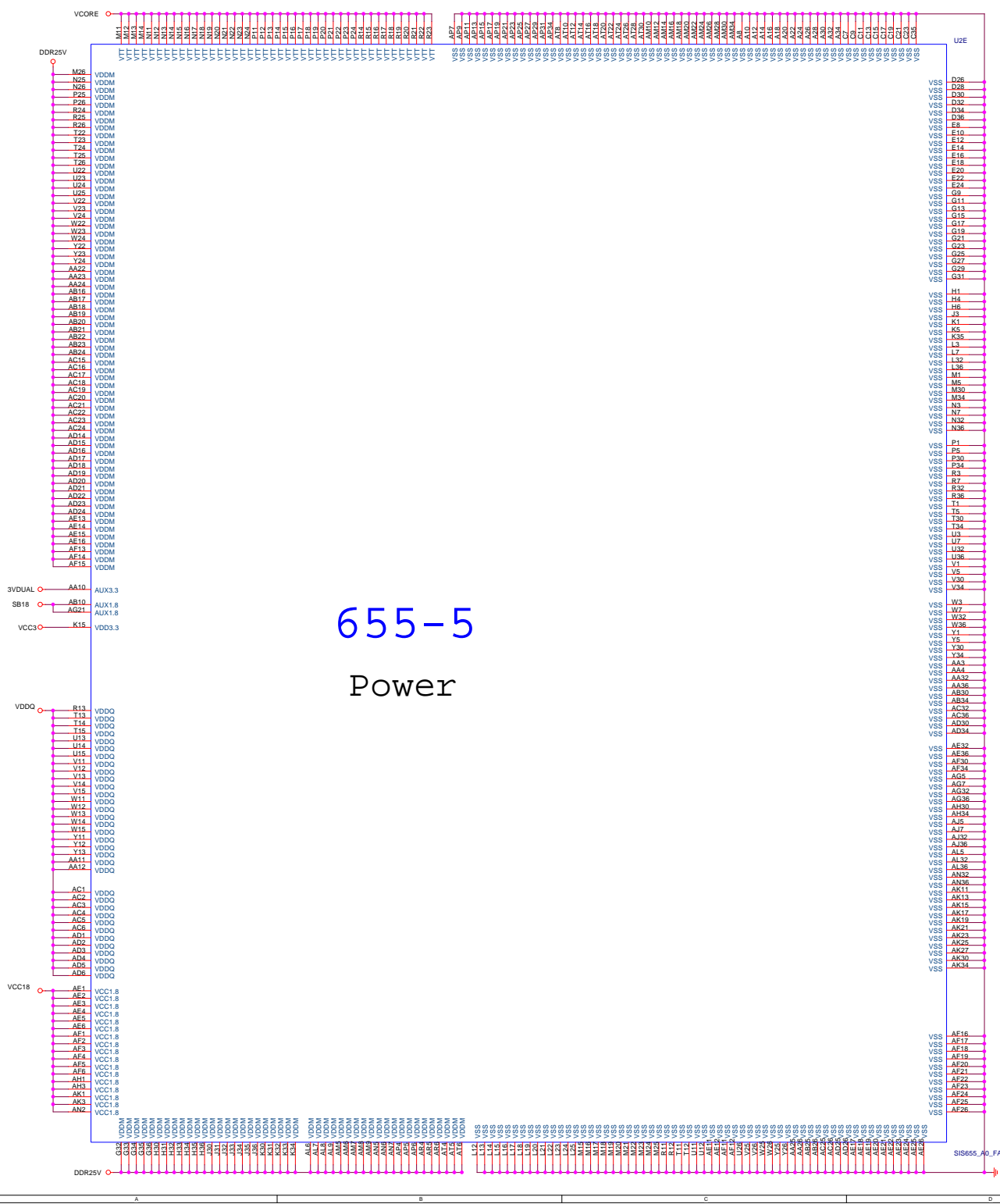
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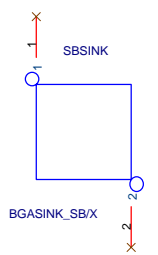
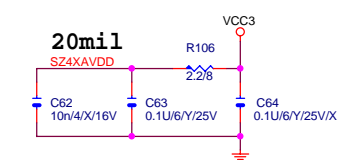
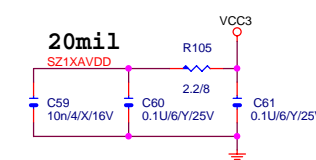
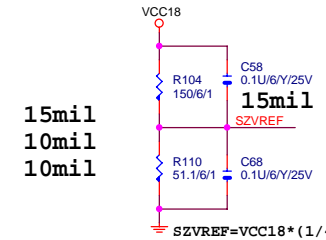
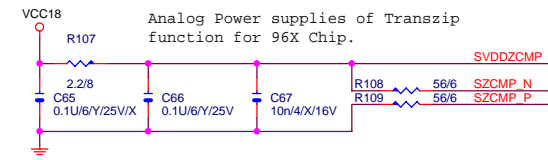
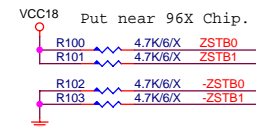
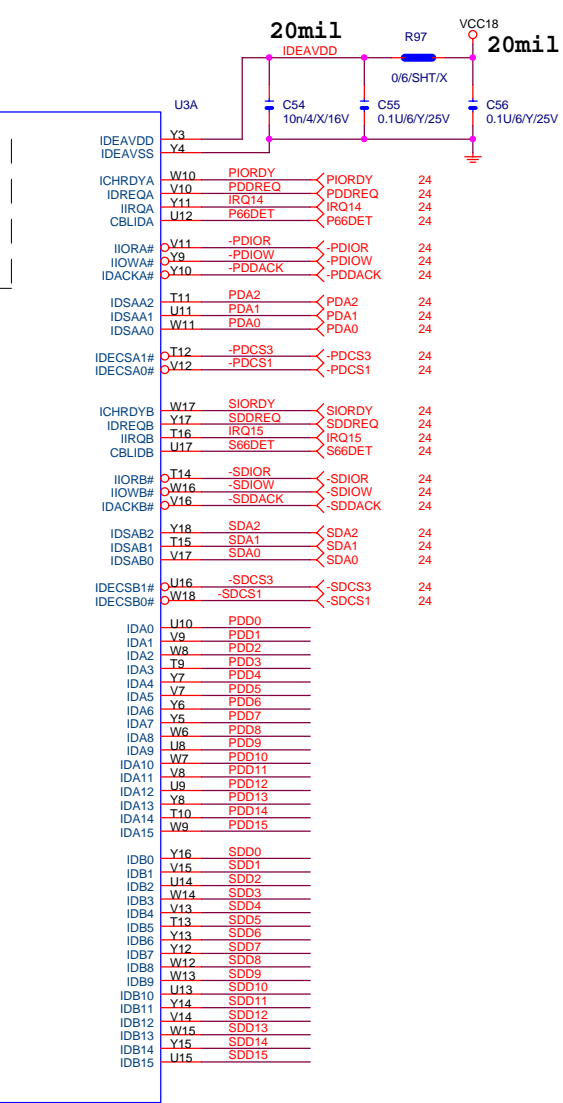
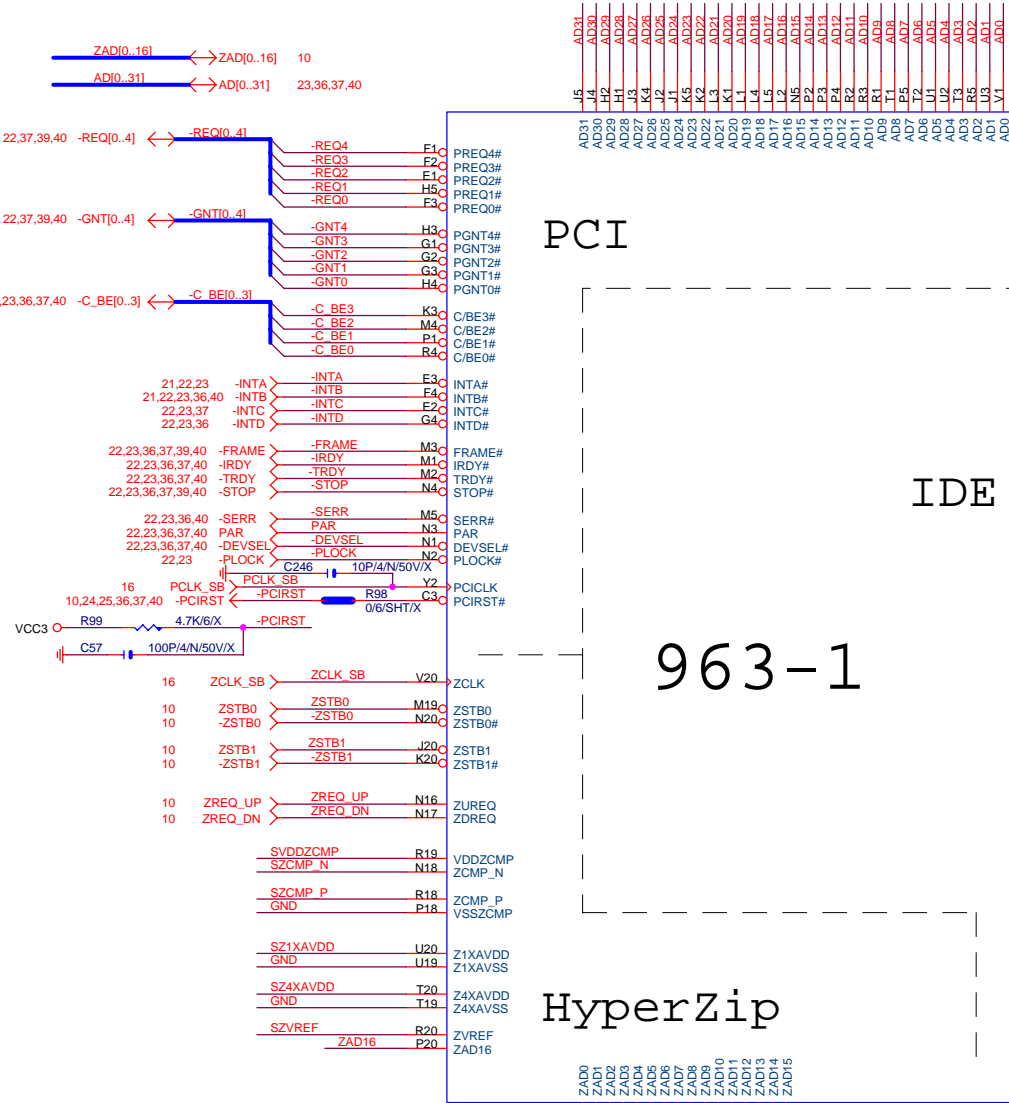


<b>GIGABYTE</b>		
Title <b>SIS648-3(HYPER ZIP)</b>		
Size Custom	Document Number <b>GA-8SQ800</b>	Rev <b>1.0</b>
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# 655-5 Power

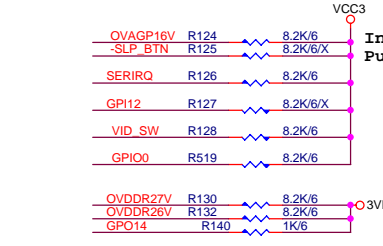
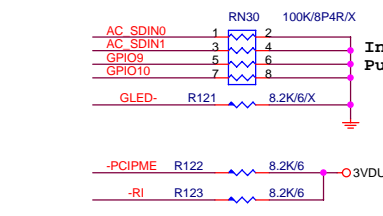
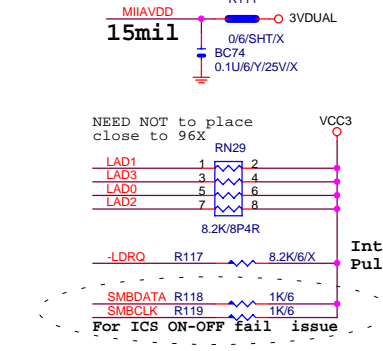
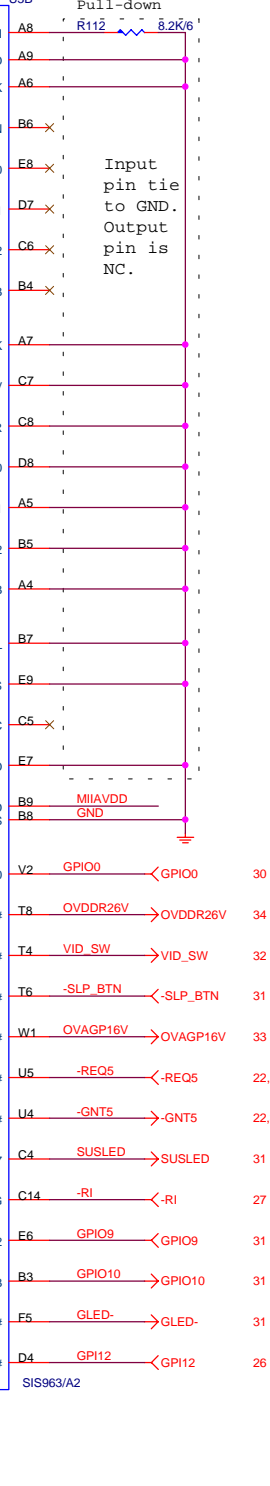
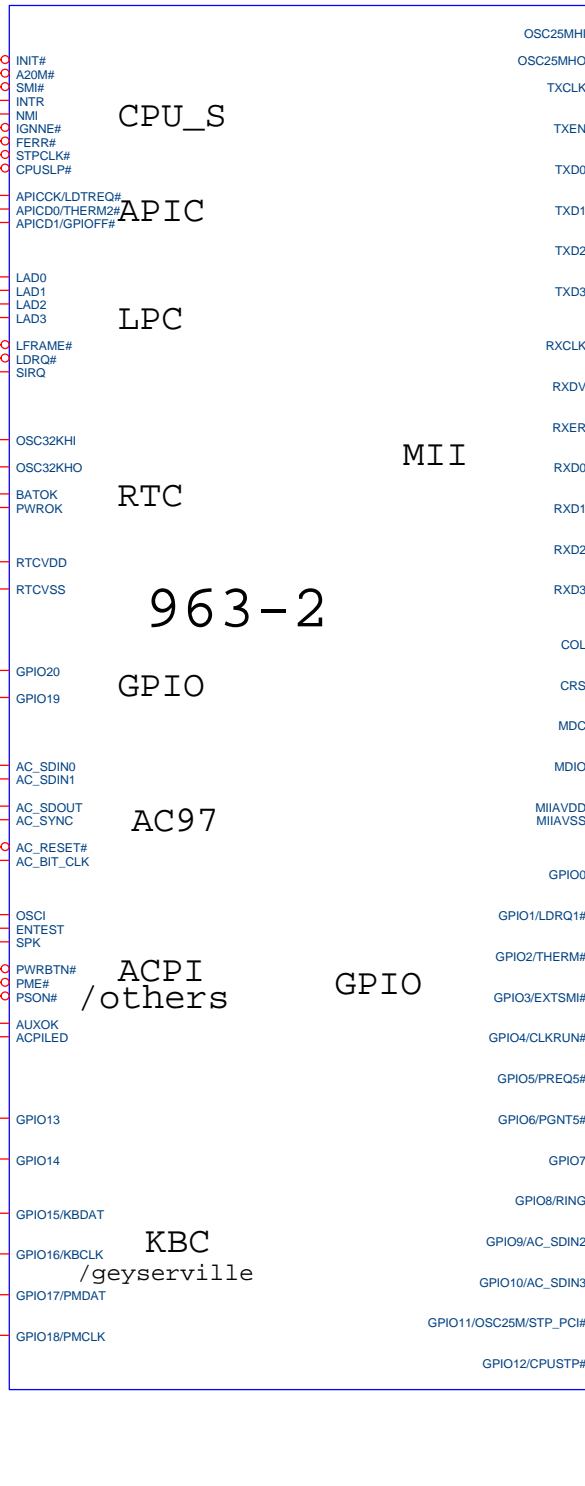
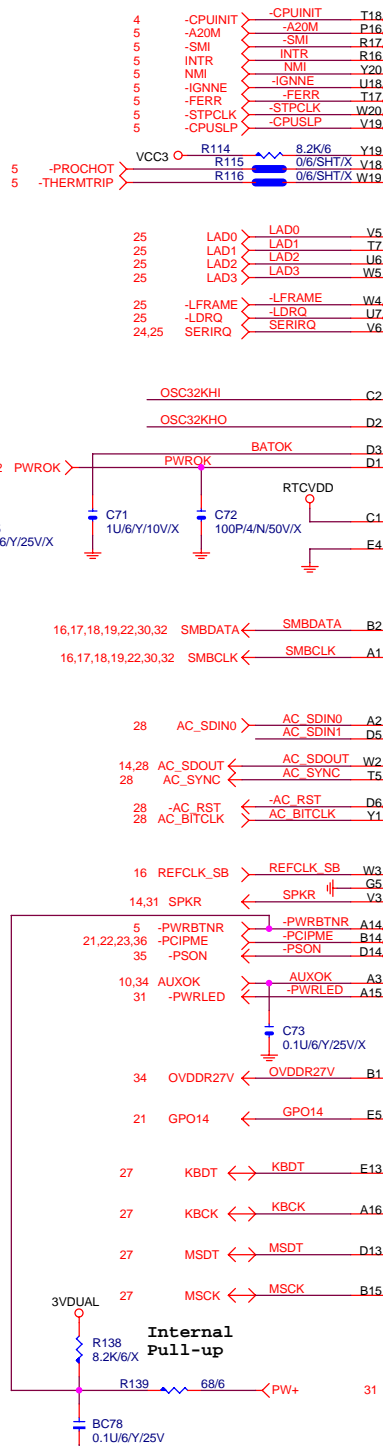


<b>GIGABYTE</b>		
<b>SIS655-5(POWER)</b>		
File	Document Number	Rev
Size		<b>1.0</b>
<b>GA-8SQ800</b>		
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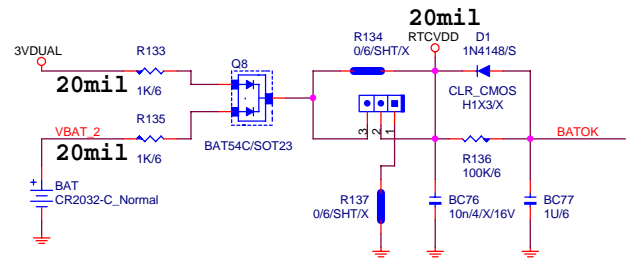


<b>GIGABYTE</b>		
<b>SIS963-1(HP ZIP,PCI,IDE)</b>		
Title	Document Number	Rev
	<b>GA-8SQ800</b>	<b>1.0</b>
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Programable on-die pull-high strength for CPU\_S:  
 ( Infinite, 150, 110, 56 Ohm)



CLR_CMOS	CLEAR COMS JUMPER
1-2	Enable
2-3	Disable (Default)



**GIGABYTE**

**SIS963-2(LPC,MII,GPIO)**

Title

Size Document Number

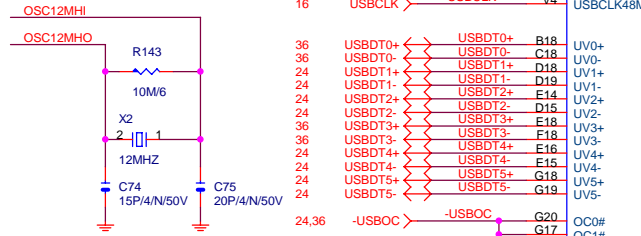
Custom

**GA-8SQ800**

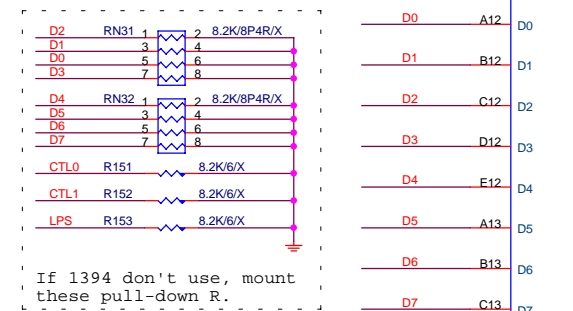
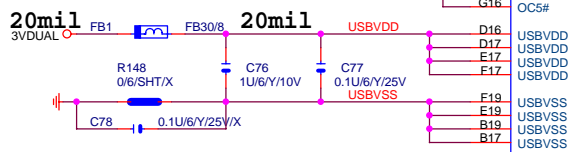
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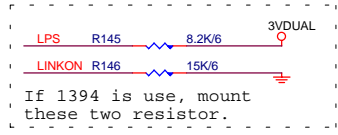
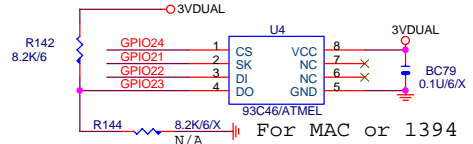
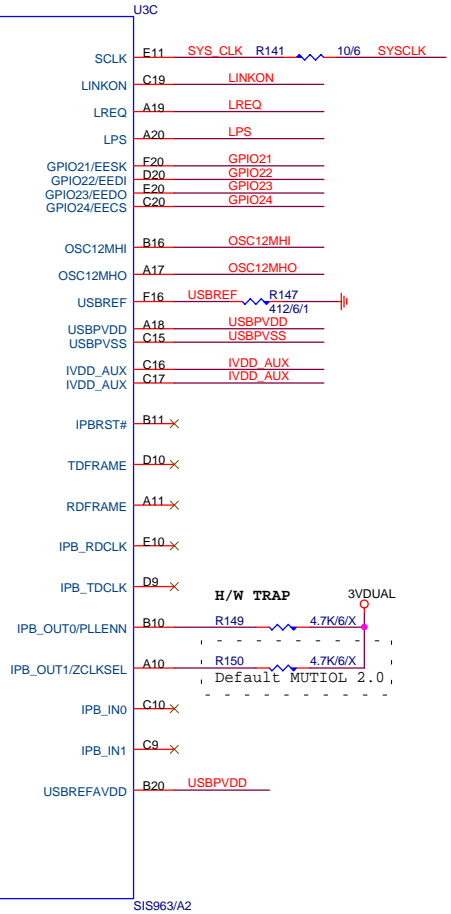
SIS963 USB 2.0



USB  
963-3



If 1394 don't use, mount these pull-down R.

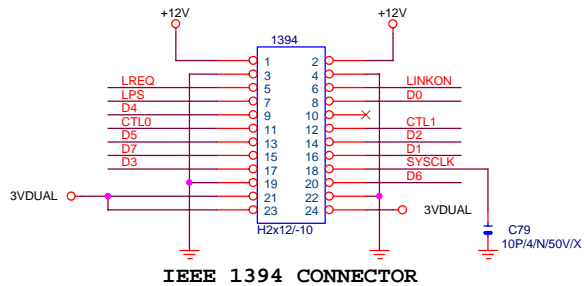


If 1394 is use, mount these two resistor.

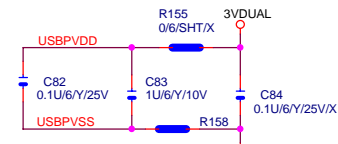
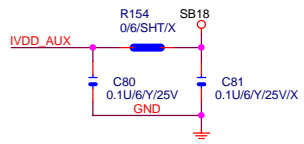
SYSCLK, LREQ, LPS, CTL[0..1], D[0..7] 須等長，相差200mil以內

	0	1	Default	
SPKR( LPC address mapping)	disable	enable	R169 un-stuff	yes
AC_SDOUT( Trap from)	ROM	PCI AD	R170 un-stuff	yes
SB debug mode	enable	disable		
	embedded pull-low (30-50K Ohm)			

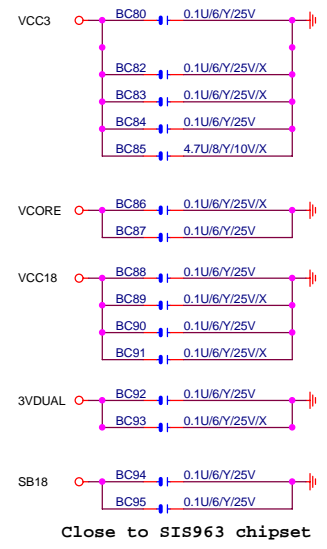
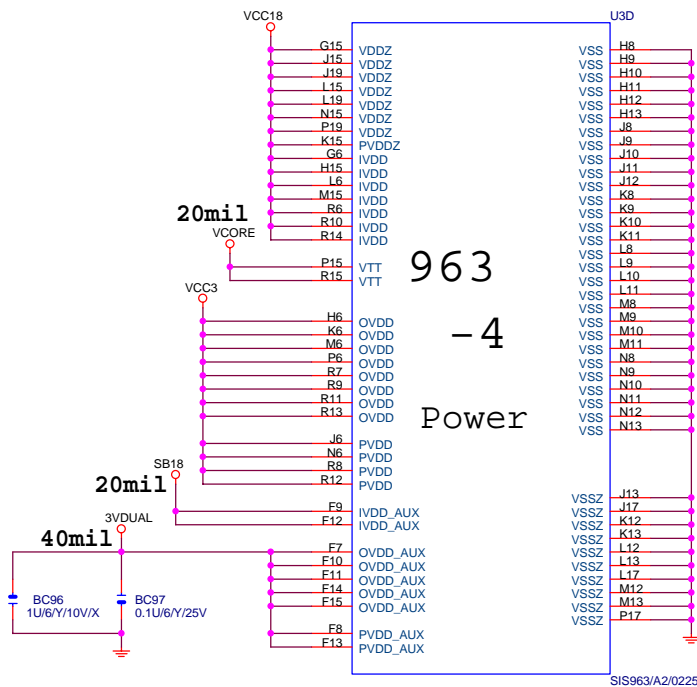
If 1394 do not use:  
Output pin(LPS, LREQ) can be open.  
All input pin pull-down to gnd.



IEEE 1394 CONNECTOR



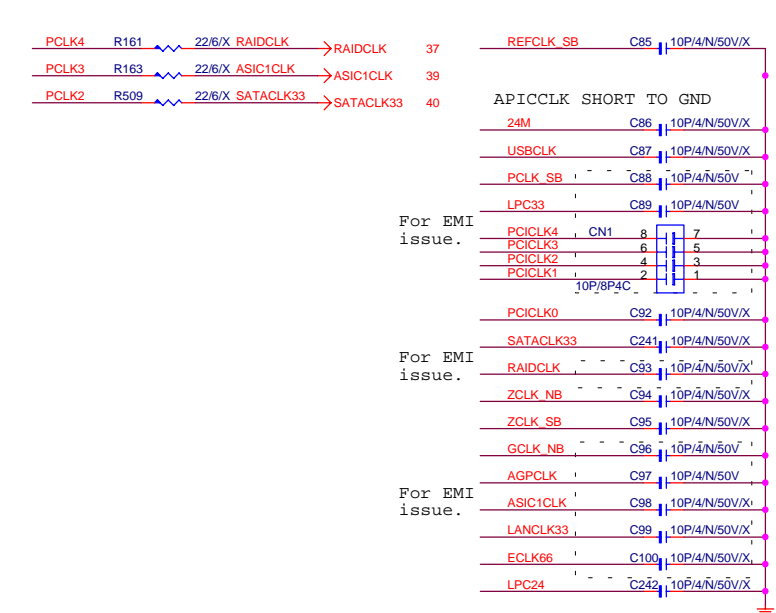
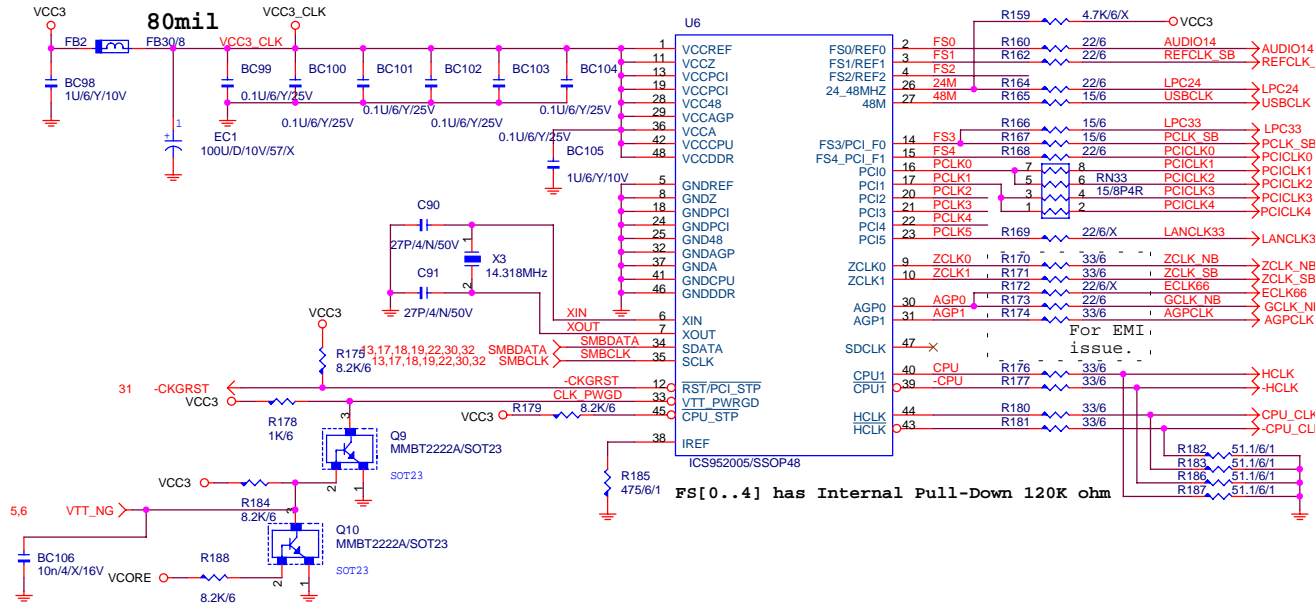
<b>GIGABYTE</b>		
<b>SIS963-3(USB2.0)</b>		
Title	Document Number	Rev
	<b>GA-8SQ800</b>	<b>1.0</b>
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**Solder side Cap.**  
 SB18 SC19 0.1U/6/Y/25V/X  
 VCC18 SC18 0.1U/6/Y/25V  
 Place on SIS963 chipset  
 Solder side.

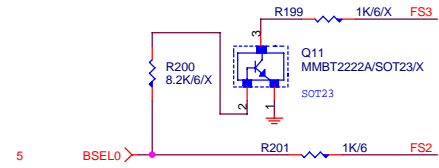
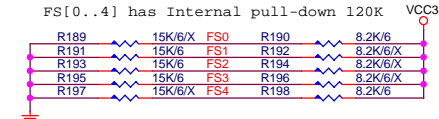
Close to SIS963 chipset

<b>GIGABYTE</b>		
Title <b>SIS963-4(POWER)</b>		
Size Custom	Document Number <b>GA-8SQ800</b>	Rev <b>1.0</b>
Date: Thursday, December 26, 2002	Sheet 15	of 40



**ICS952005/CY28381 CLOCK BOM OPTION TABLE**

H/W Strap	R190	R196	R198	R201	R200	Q11	R199
ICS952005 100.2/133.6	8.2K	N/A	8.2K	1K	N/A	N/A	N/A
CY28381 100.0/133.9	8.2K	8.2K	N/A	1K	8.2K	MMBT 2222	1K



ICS952005

FS4	FS3	FS2	FS1	FS0	CPU	DDR	AGP	ZCLK
1	0	0	0	1	100.2	133.6	66.8	133.6
1	0	1	0	1	133.6	133.6	66.8	133.6

CY28381

FS4	FS3	FS2	FS1	FS0	CPU	DDR	AGP	ZCLK
0	1	0	0	1	100.0	133.33	66.67	133.3
0	0	1	0	1	133.9	133.9	66.95	133.9

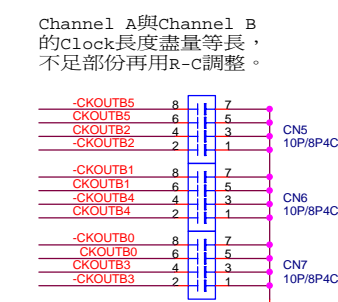
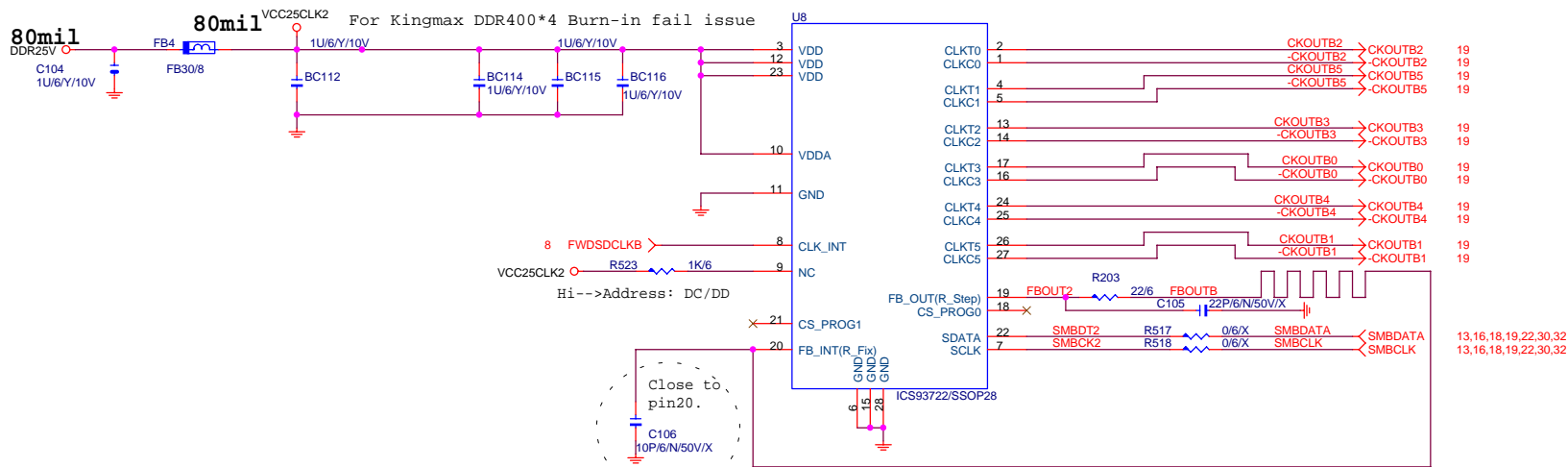
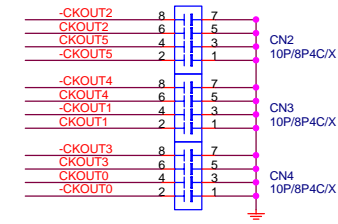
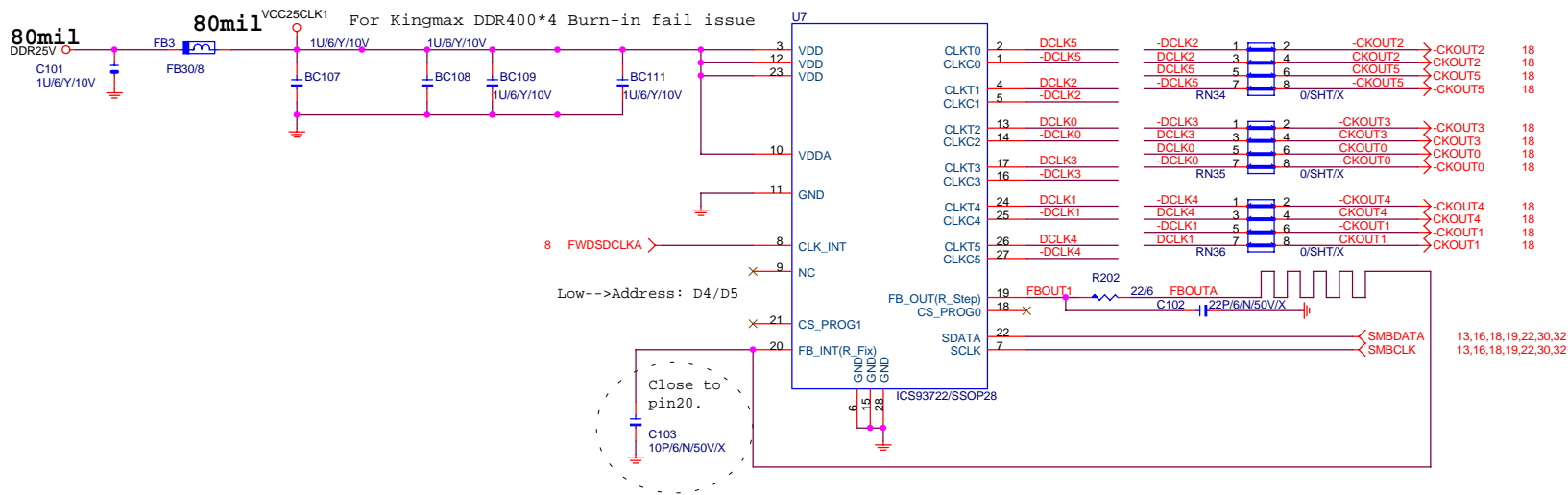
**GIGABYTE**

**CLOCK GEN + SDR BUFFER**

Size Custom Document Number **GA-8SQ800** Rev **1.0**

Date: Thursday, December 26, 2002 Sheet 16 of 40

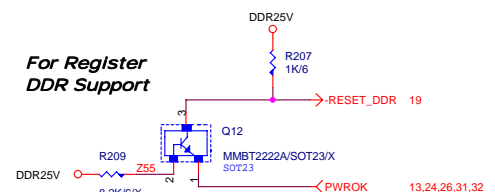
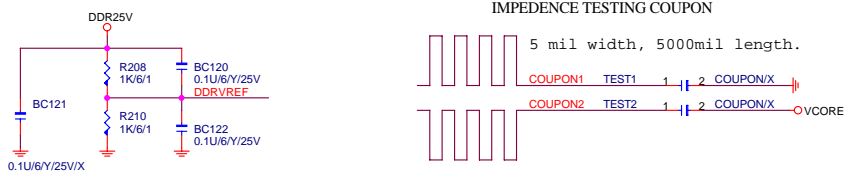
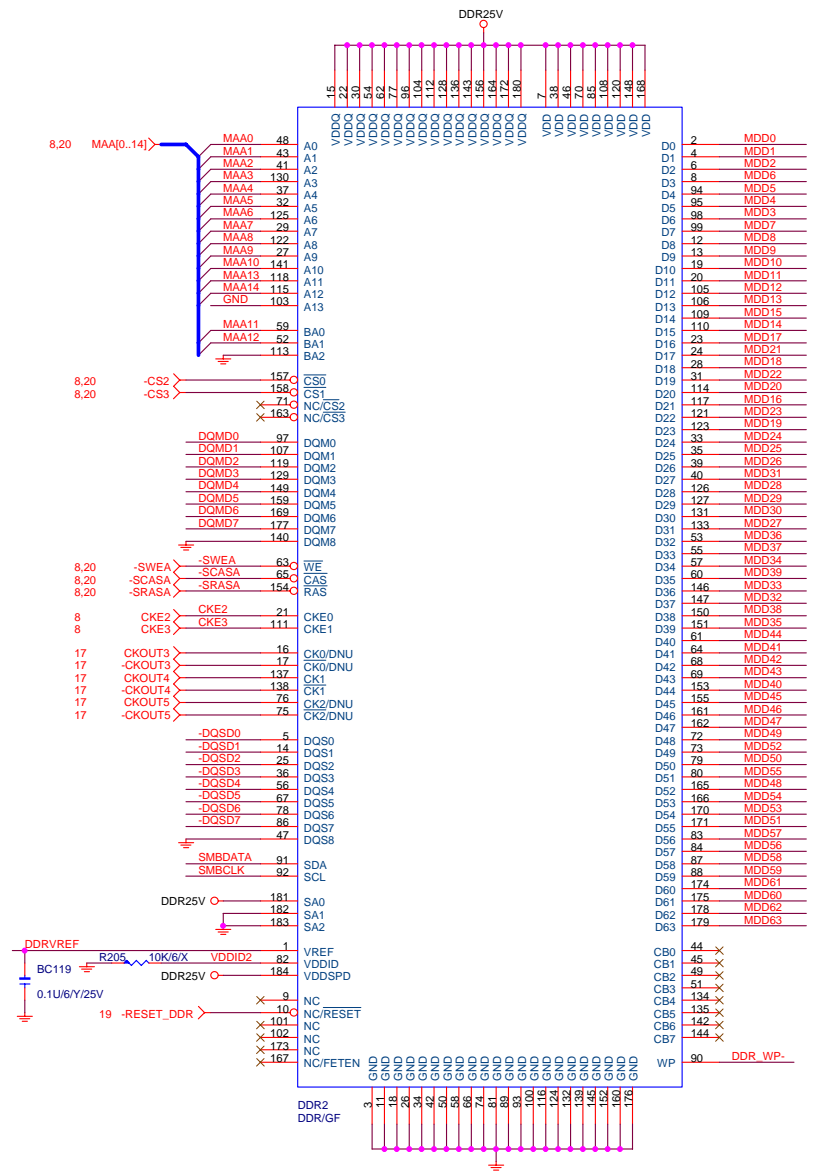
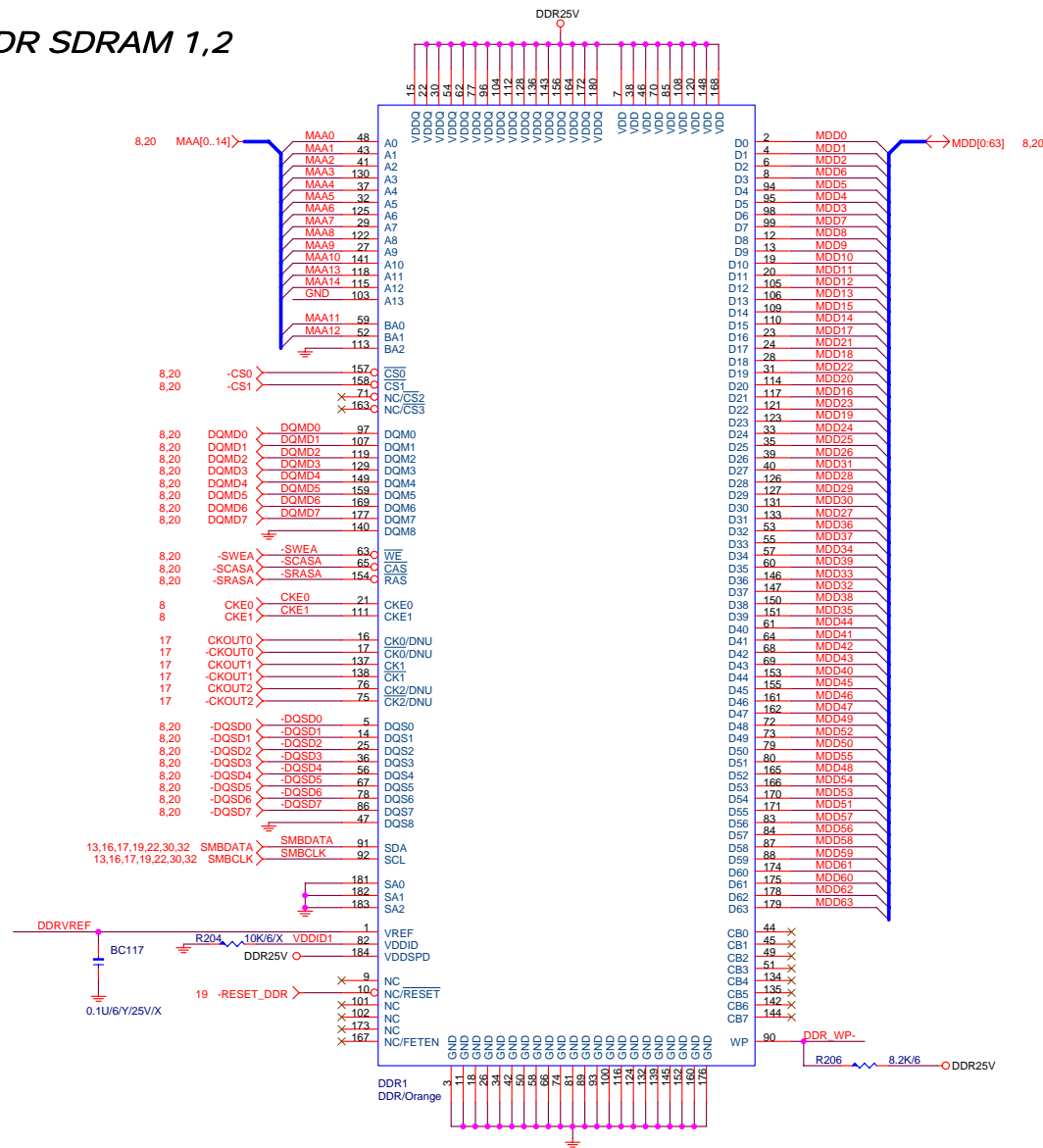




Channel A與Channel B  
的Clock長度盡量等長，  
不足部份再用r-c調整。

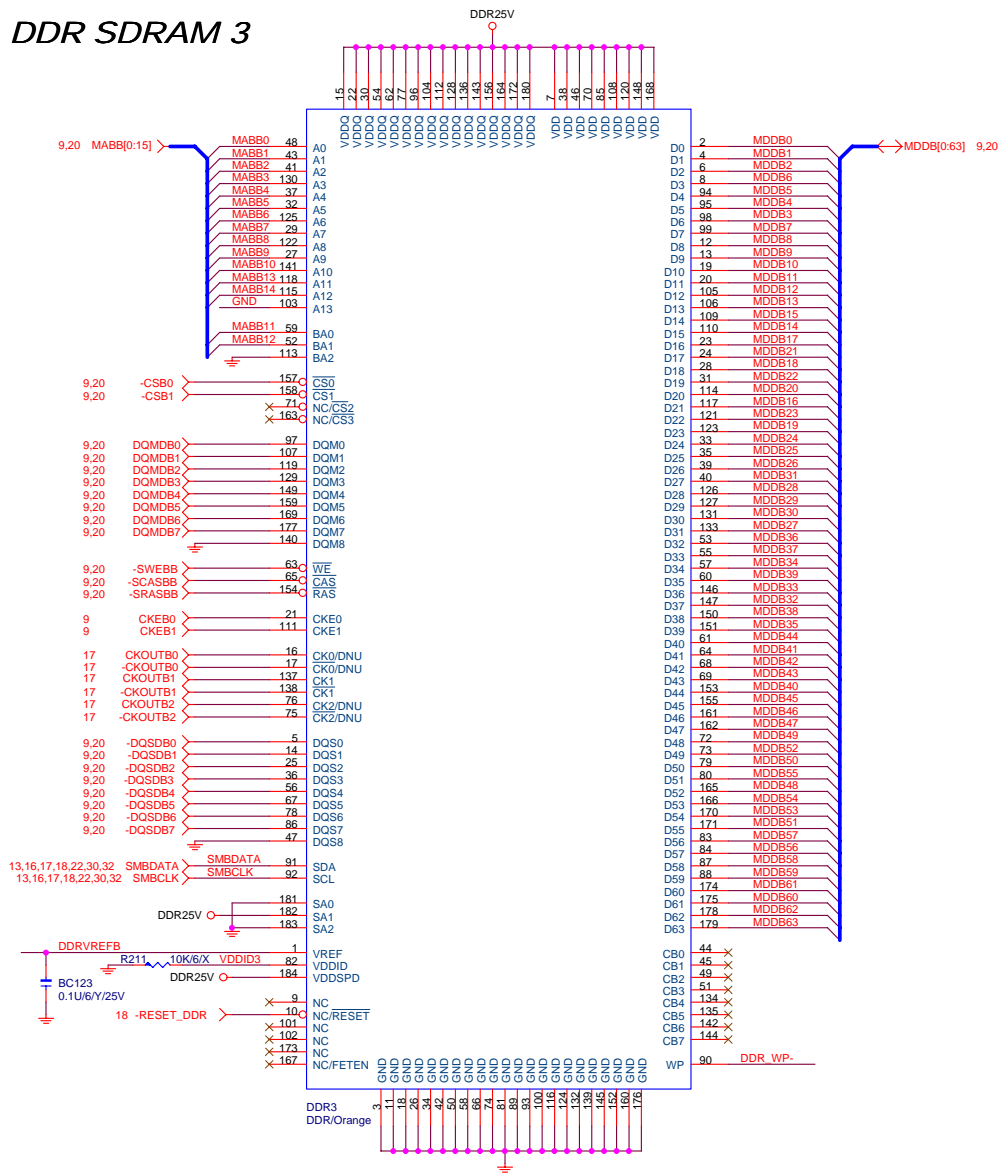
<b>GIGABYTE</b>		
<b>DDR CLOCK BUFFER</b>		
Title		
Size	Document Number	Rev
Custom	<b>GA-8SQ800</b>	<b>1.0</b>
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# DDR SDRAM 1,2

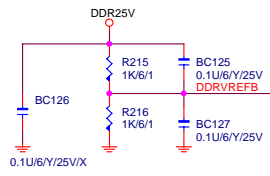
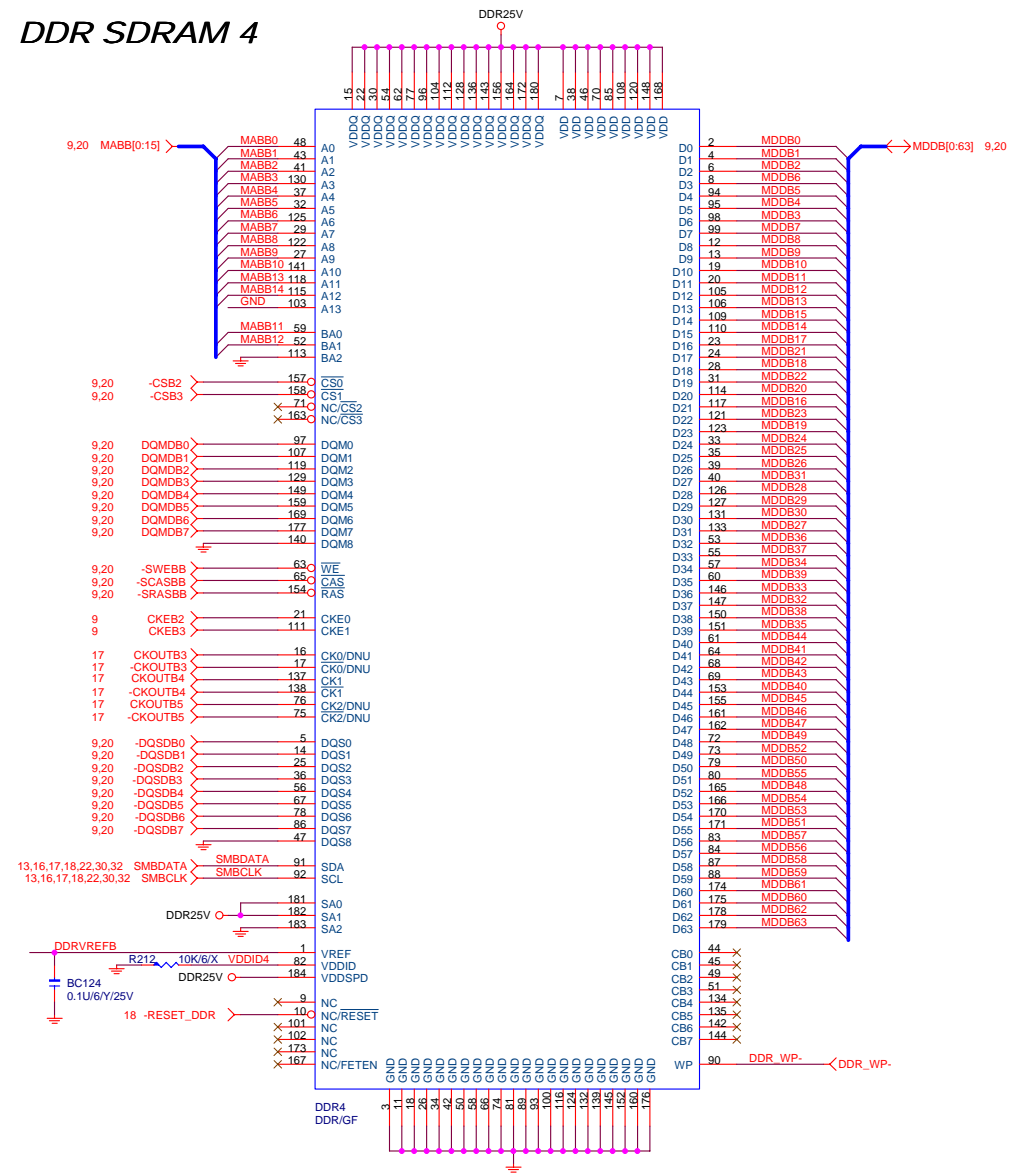


<b>GIGABYTE</b>		
<b>DDR UNBUFFERED 1,2</b>		
Title	Document Number	Rev
	<b>GA-8SQ800</b>	<b>1.0</b>
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# DDR SDRAM 3

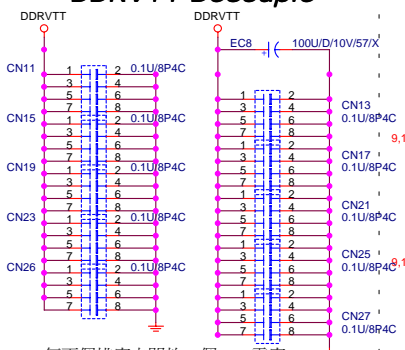


# DDR SDRAM 4

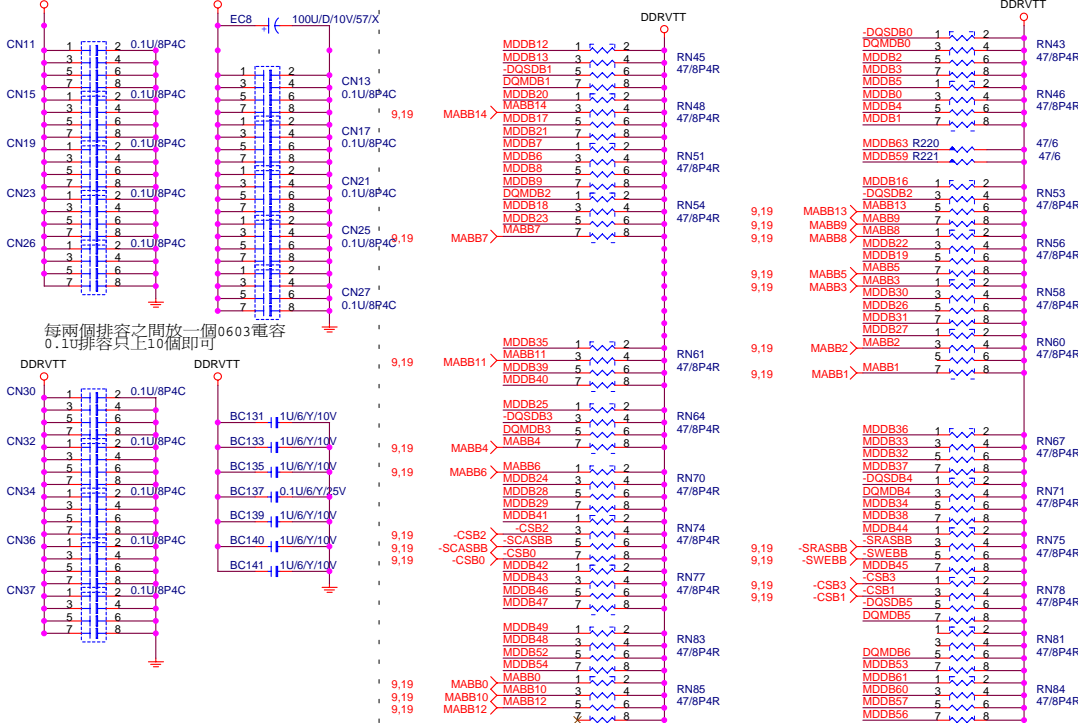


<b>GIGABYTE</b>		
<b>DDR UNBUFFERED 3,4</b>		
Size	Document Number	Rev
Custom	<b>GA-8SQ800</b>	<b>1.0</b>
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### DDRVTT Decouple

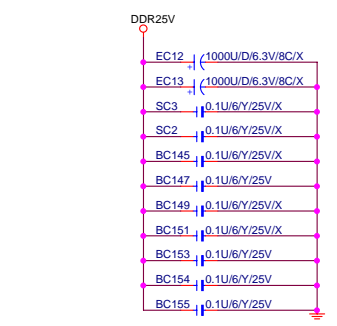


### DDR 3,4 TERMINATION



NOTE: Place these decoupling capacitors close to VTT\_MEM termination resistors. (one decoupling capacitor for each two R-packs)

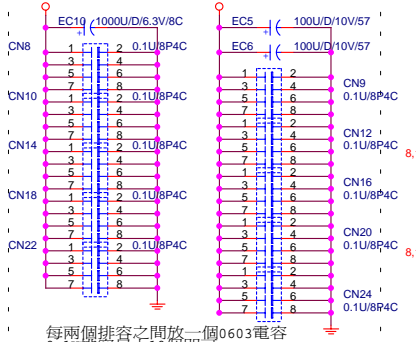
### DDR25V Decouple



HCLK & -HCLK Decoupling Cap.

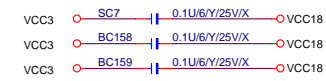
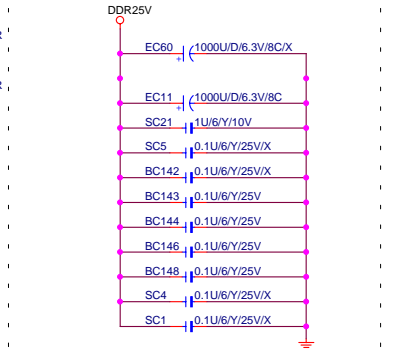


### DDRVTT Decouple

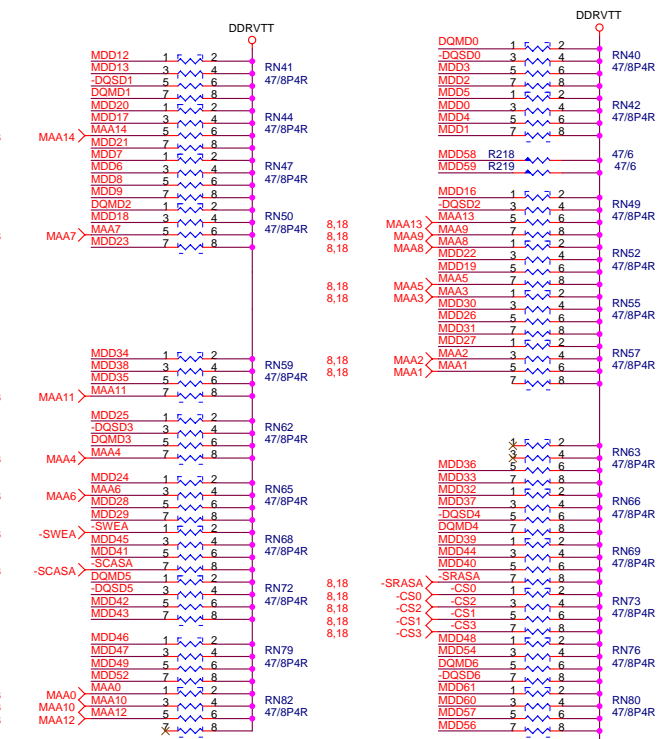


NOTE: Place these decoupling capacitors close to VTT\_MEM termination resistors. (one decoupling capacitor for each two R-packs)

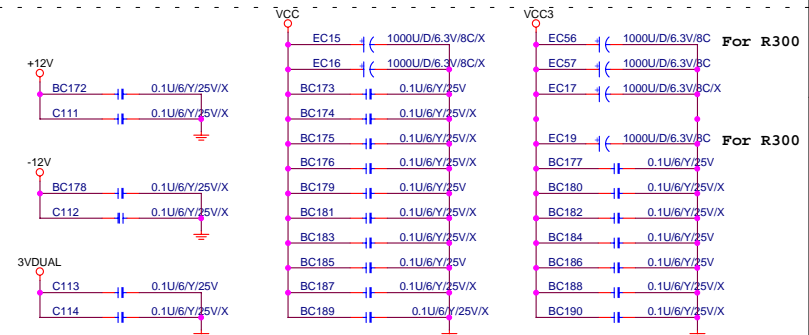
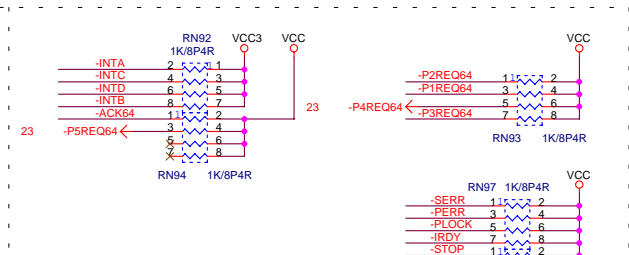
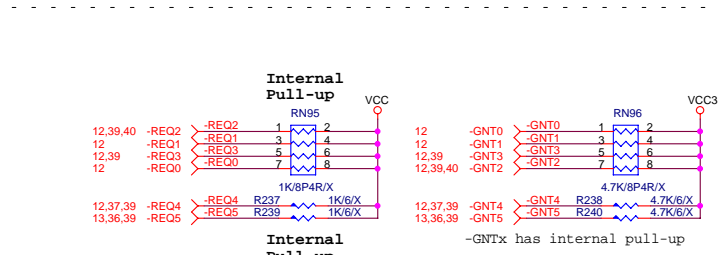
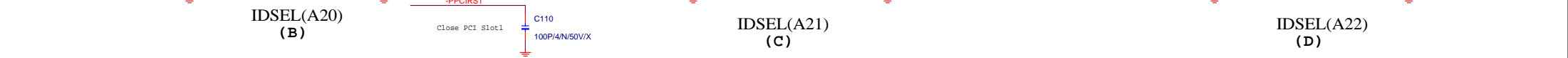
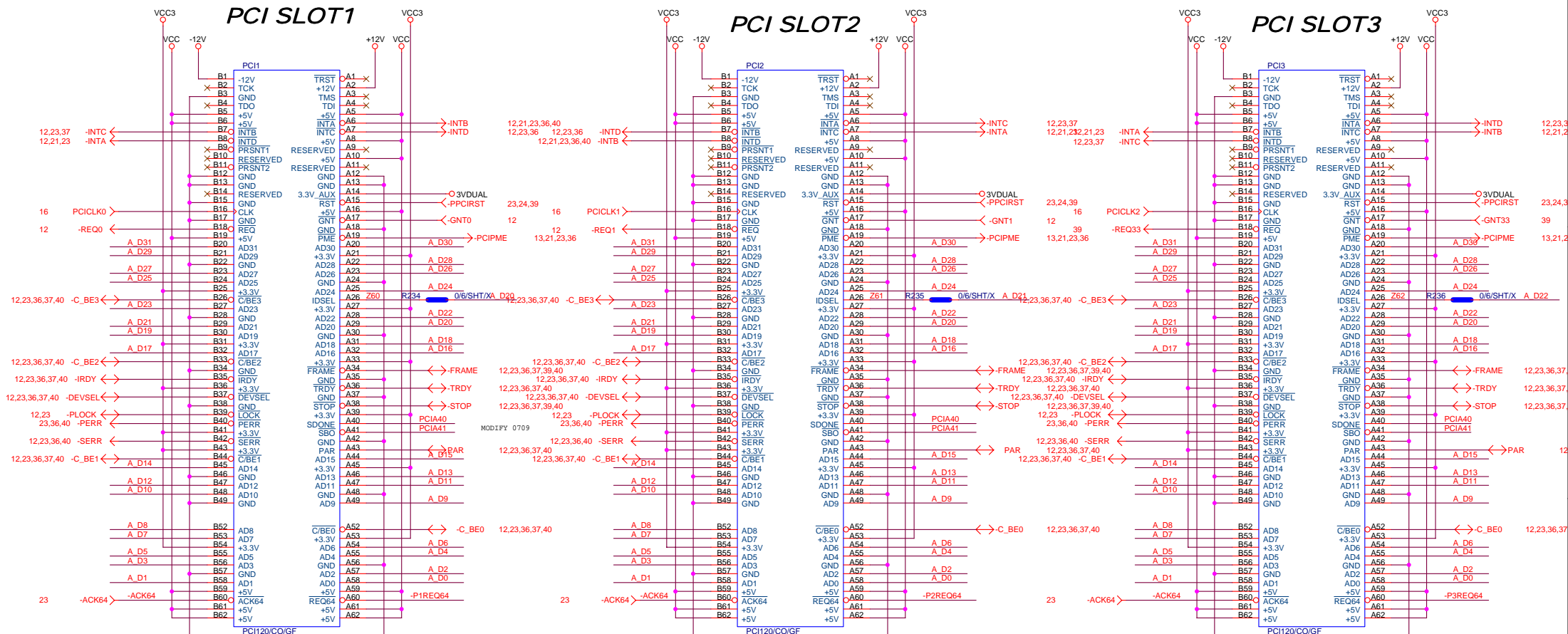
### DDR25V Decouple



### DDR 1,2 TERMINATION

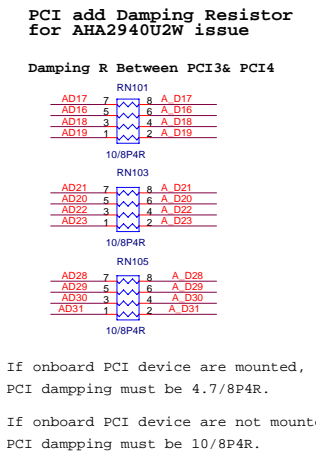
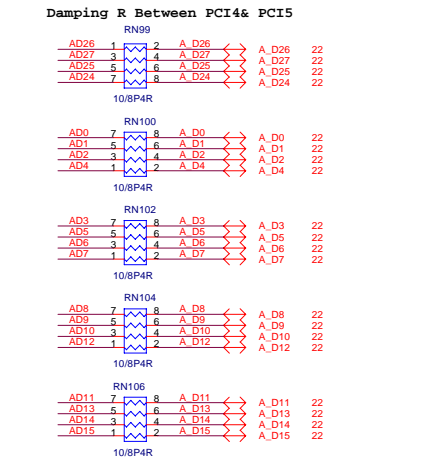
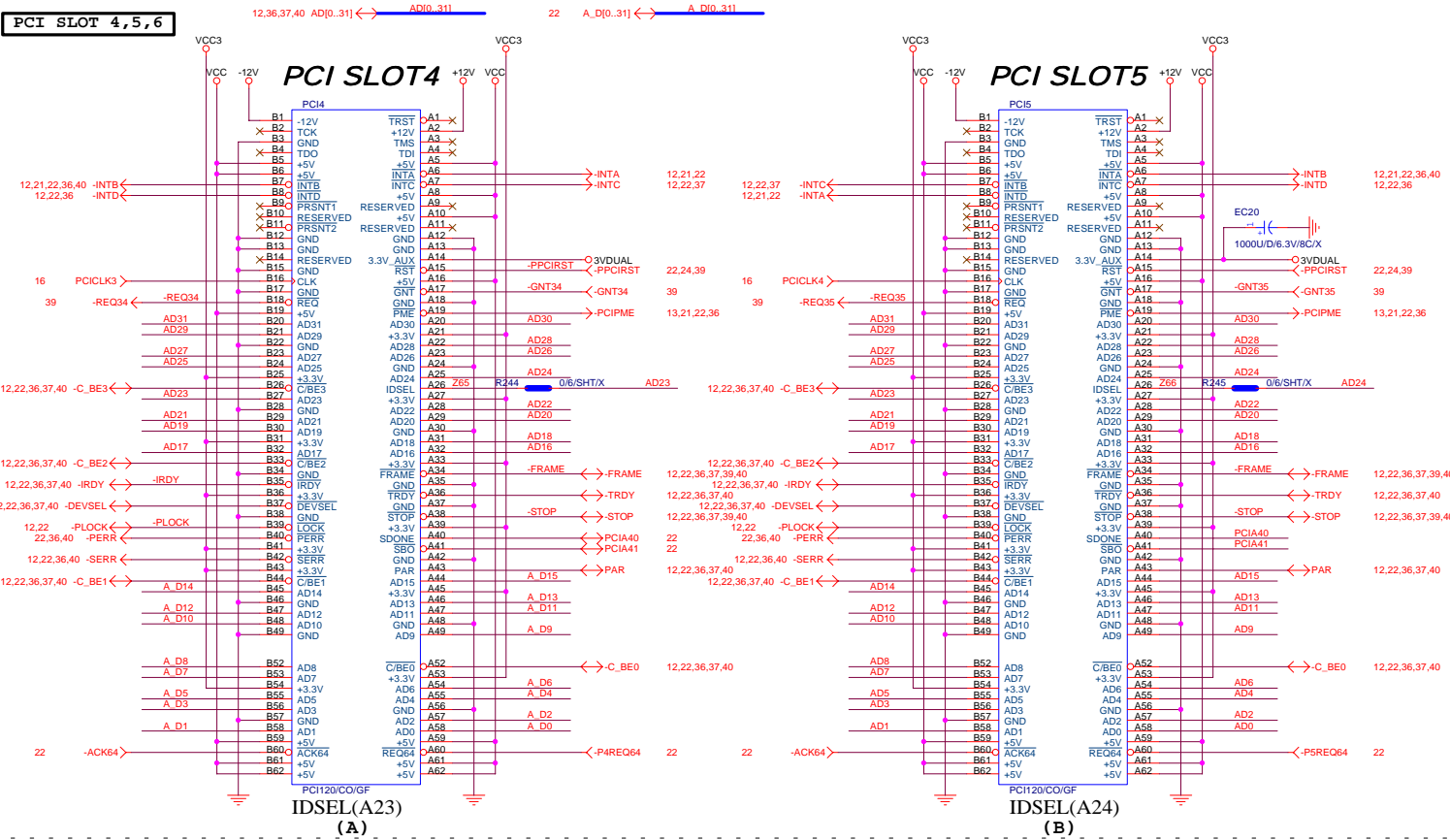






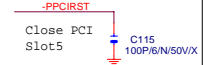


PCI SLOT 4,5,6



If onboard PCI device are mounted,  
PCI damping must be 4.7/8P4R.

If onboard PCI device are not mounted,  
PCI damping must be 10/8P4R.



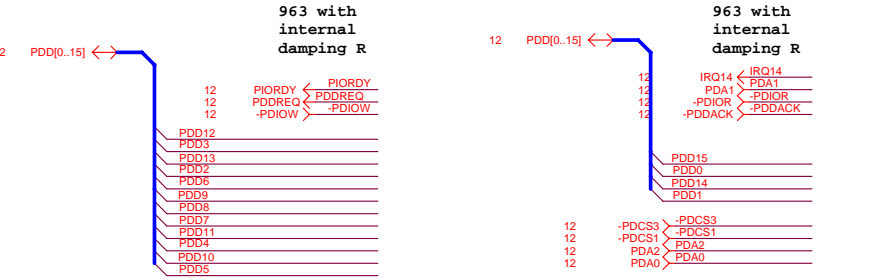
文字面秀 AGP8X & DDR400 & Dual Channel DDR

**GIGABYTE**

**PCI SLOT 4, 5**

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Size	GA-8SQ800		1.0
Customer	Date: Thursday, December 26, 2002		Sheet 23 of 40

**PRIMARY IDE**

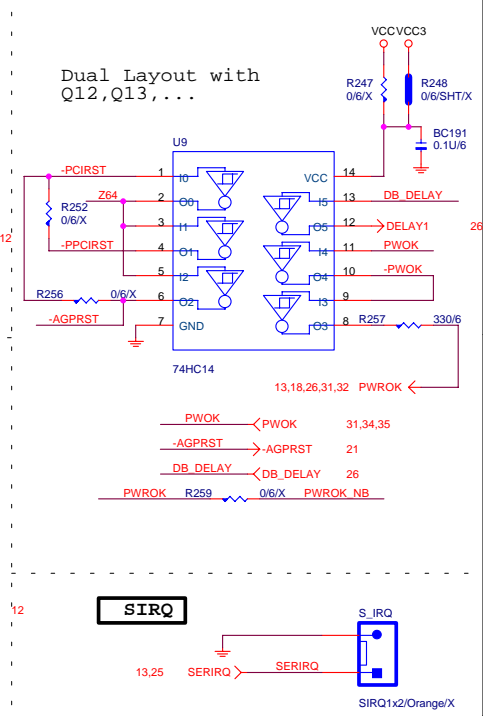
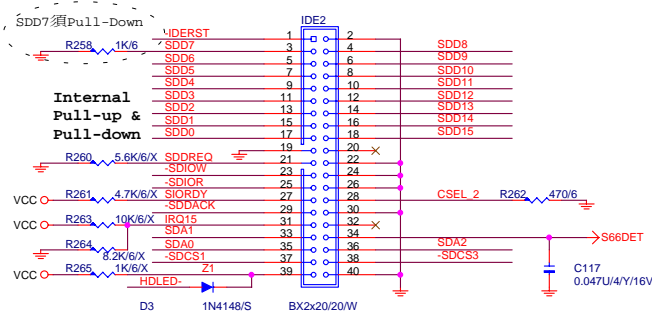
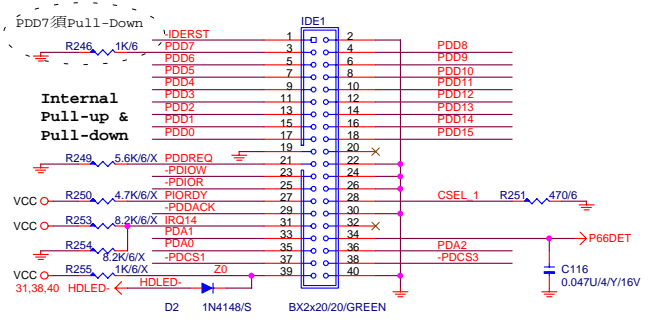


These resistor should placed near South Bridge

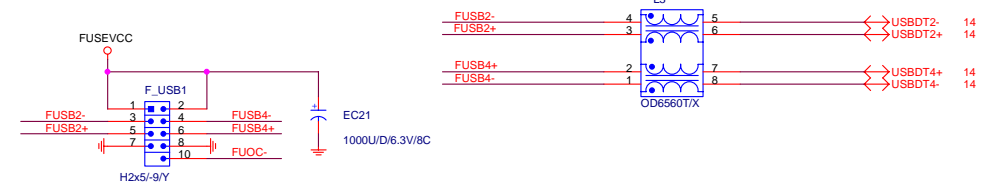
**SECONDARY IDE**



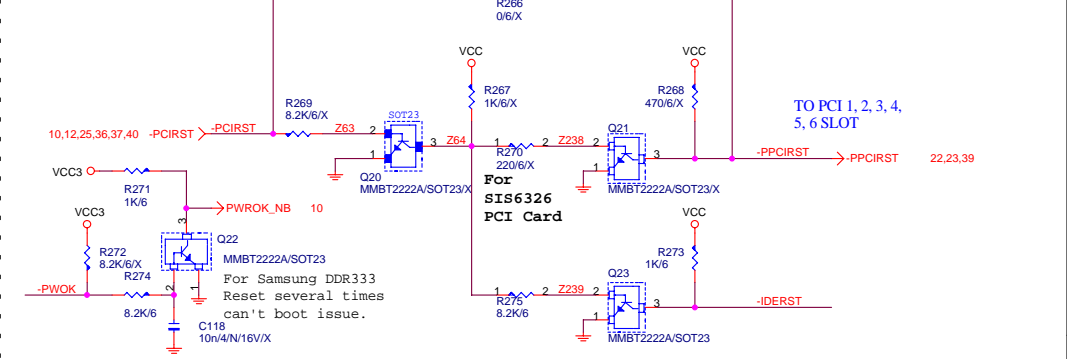
These resistor should placed near South Bridge



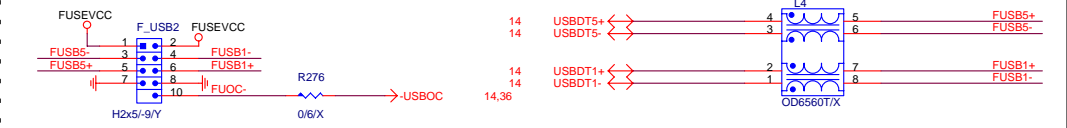
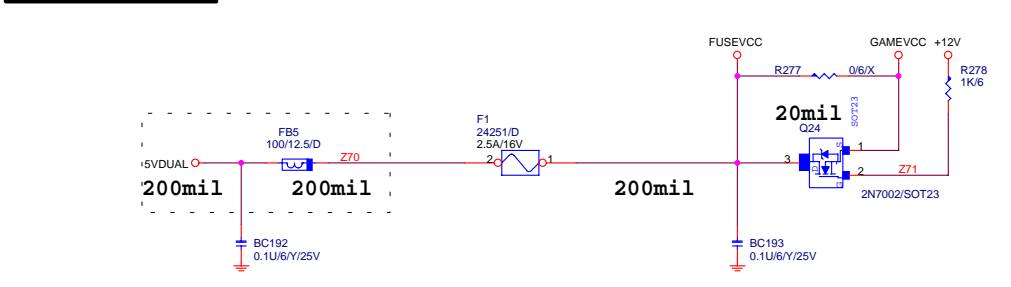
**FRONT SIDE USB1**



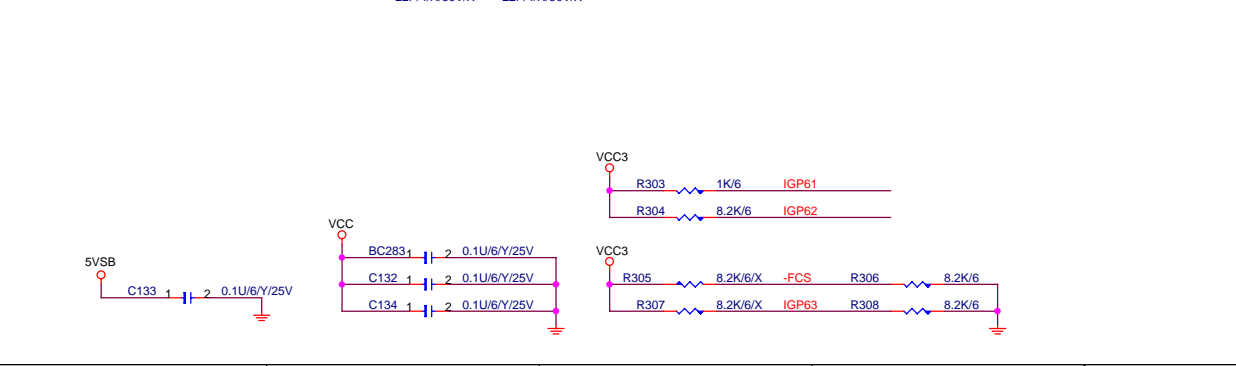
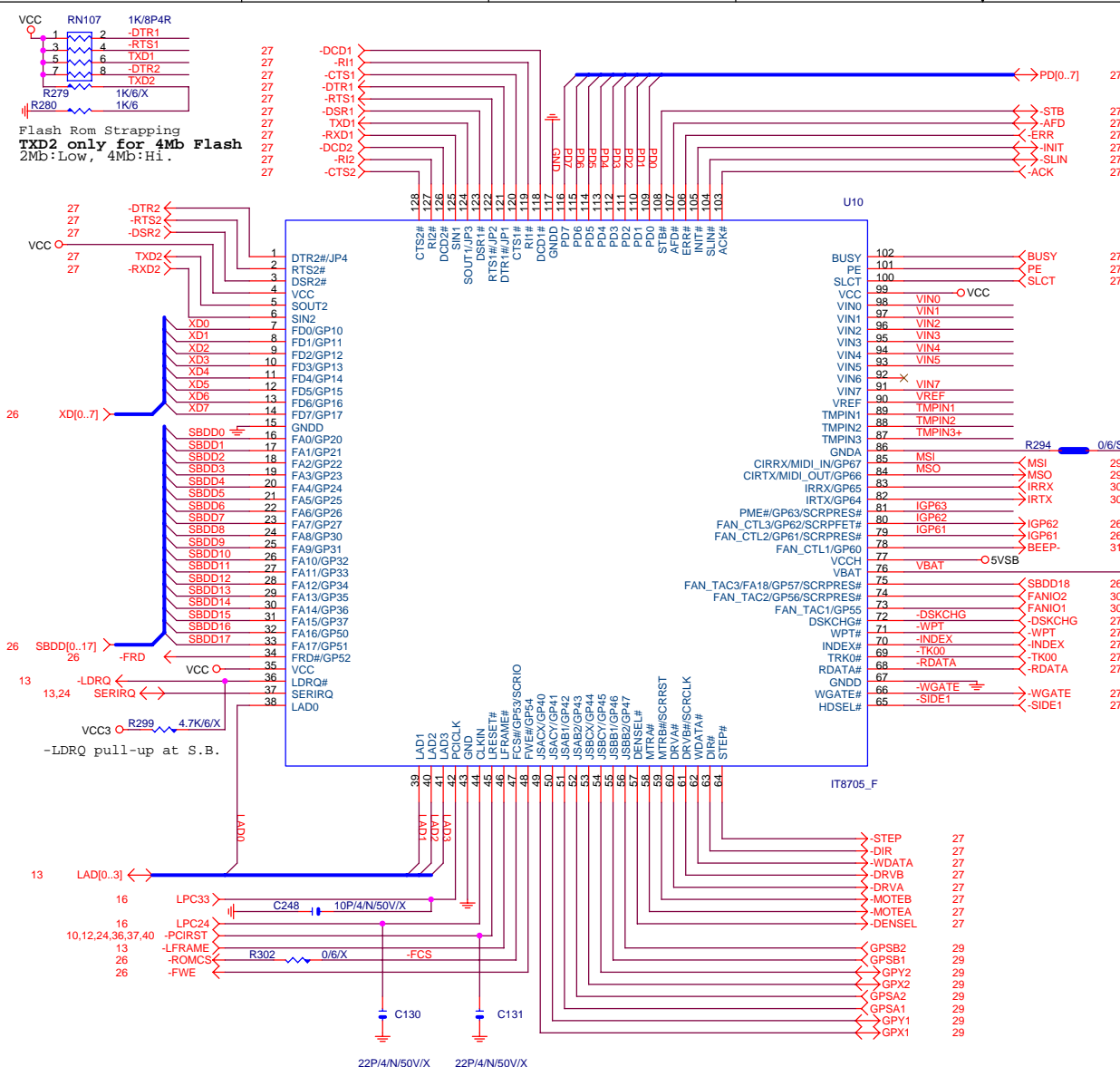
**PCI+IDE RESET**



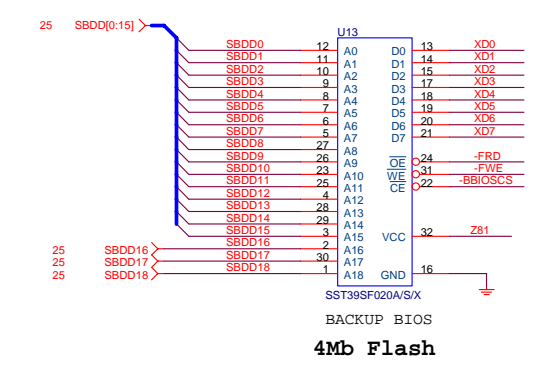
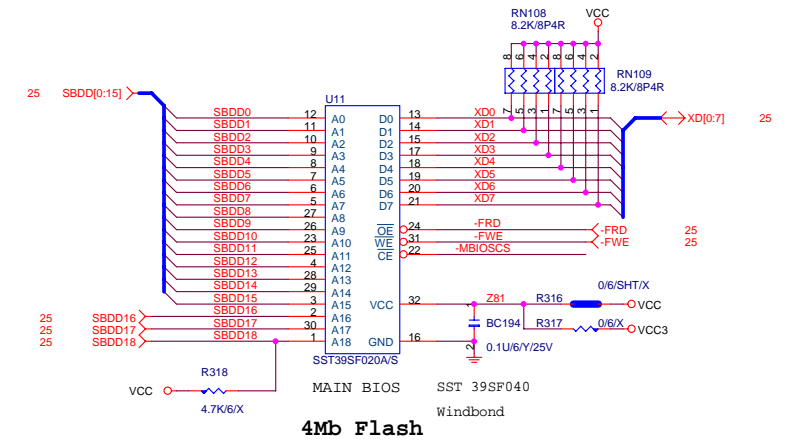
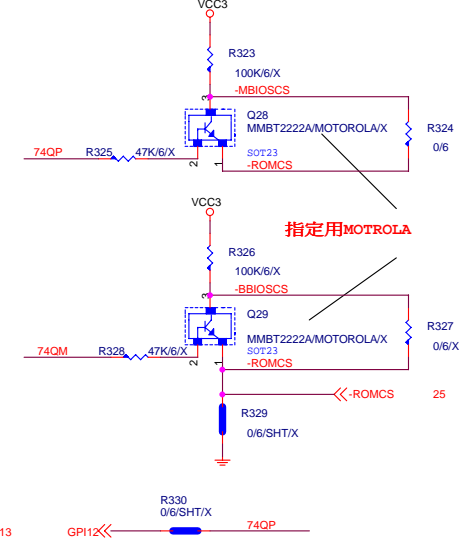
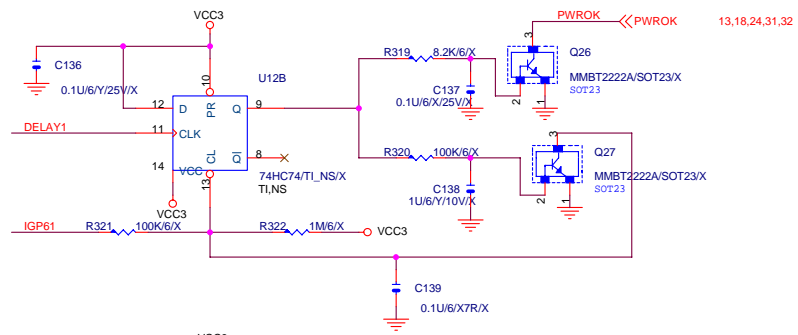
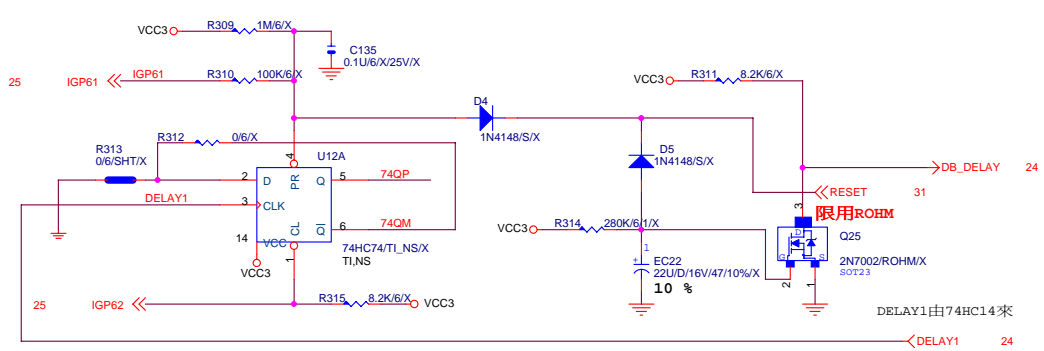
**FUSEVCC, GAMEVCC**







<b>GIGABYTE</b>	
<b>LPC I/O IT8705</b>	
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Rev	1.0



DUAL BIOS SELECTION

	Main	Backup
GPIO61	0	1
GPIO62	1	0

**GIGABYTE**

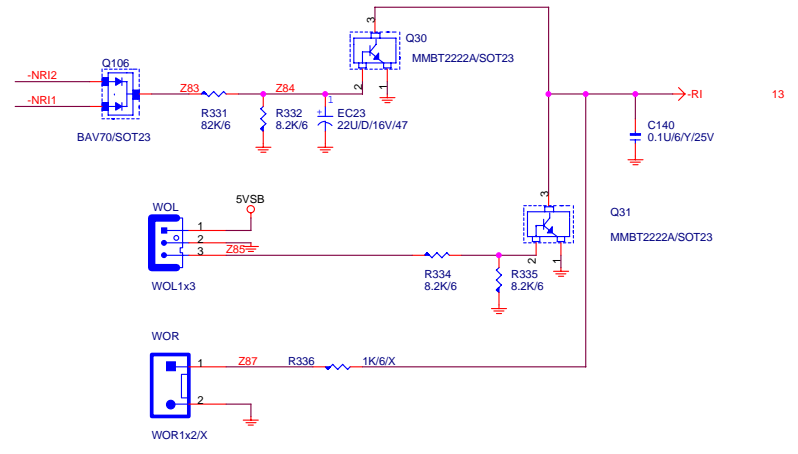
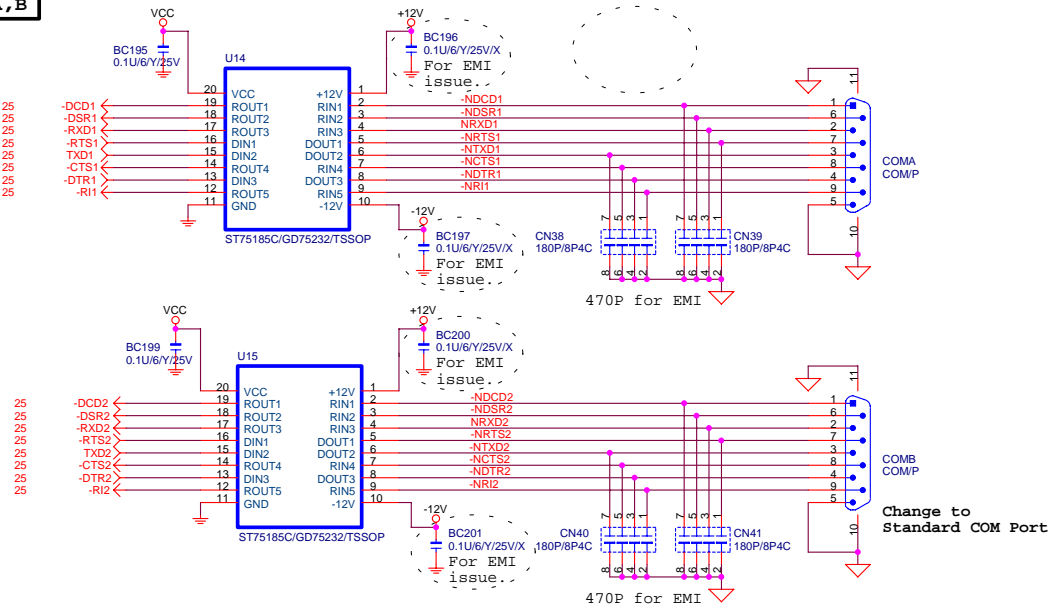
**DUAL BIOS**

Title

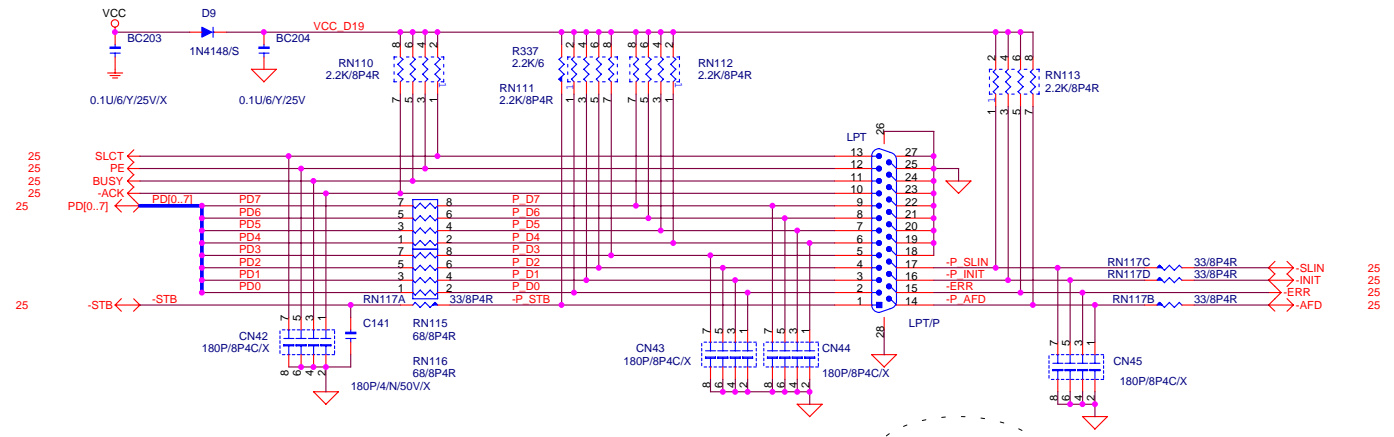
Size Custom Document Number **GA-8SQ800** Rev **1.0**

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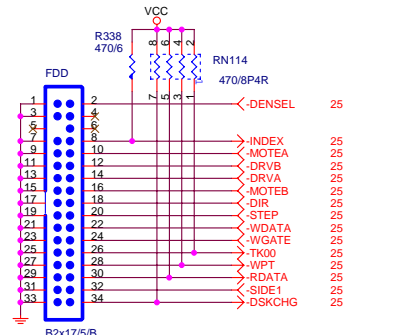
**COM A, B**



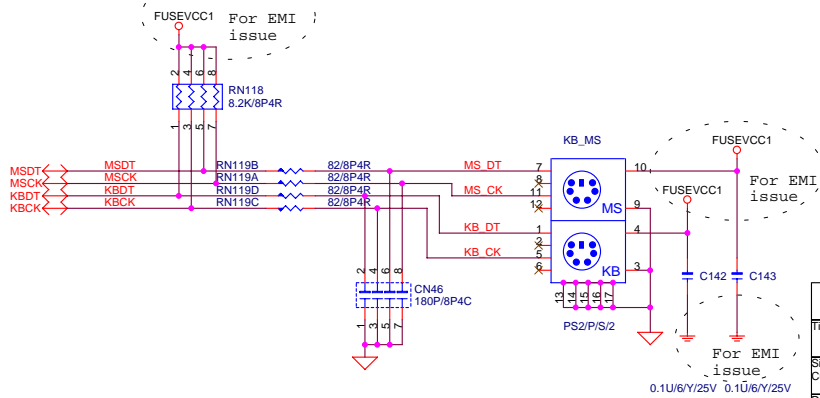
**LPT**



**FDD**

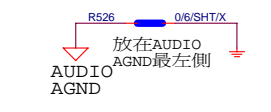
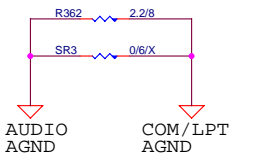
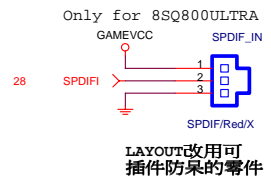
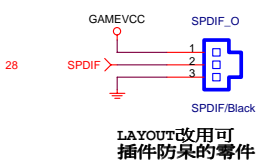


**KBC/PS2**

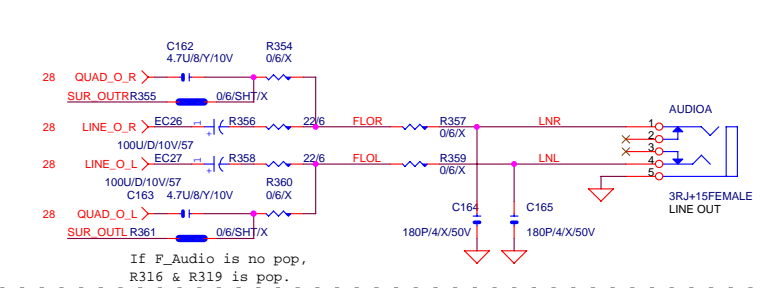




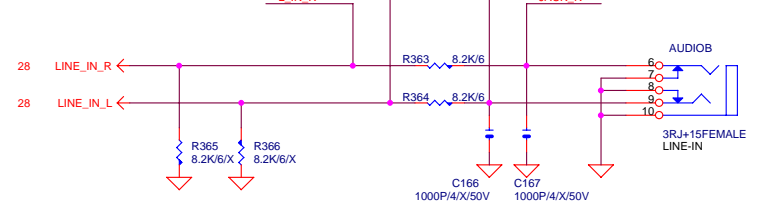
### SPDIF



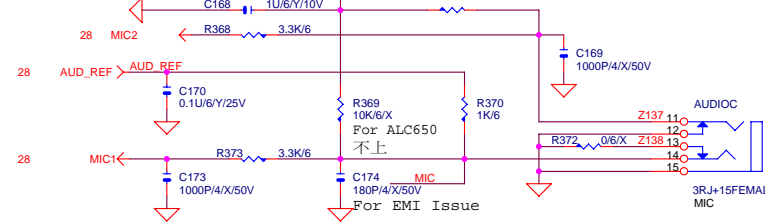
### LINE OUT



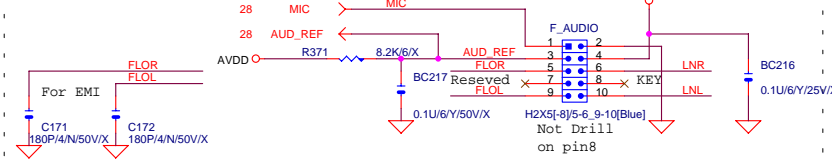
### LINE-IN



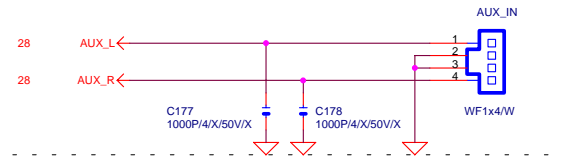
### MIC



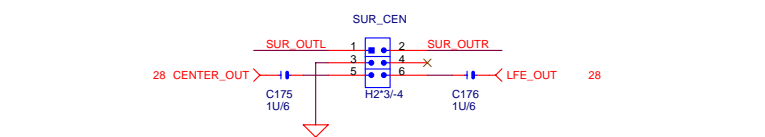
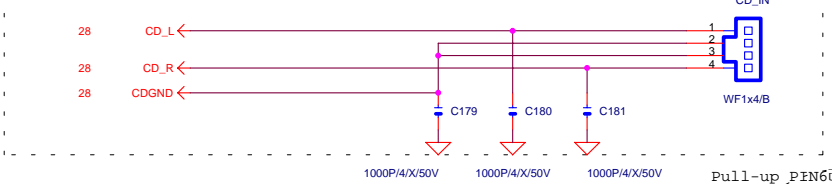
### INTEL FRONT AUDIO



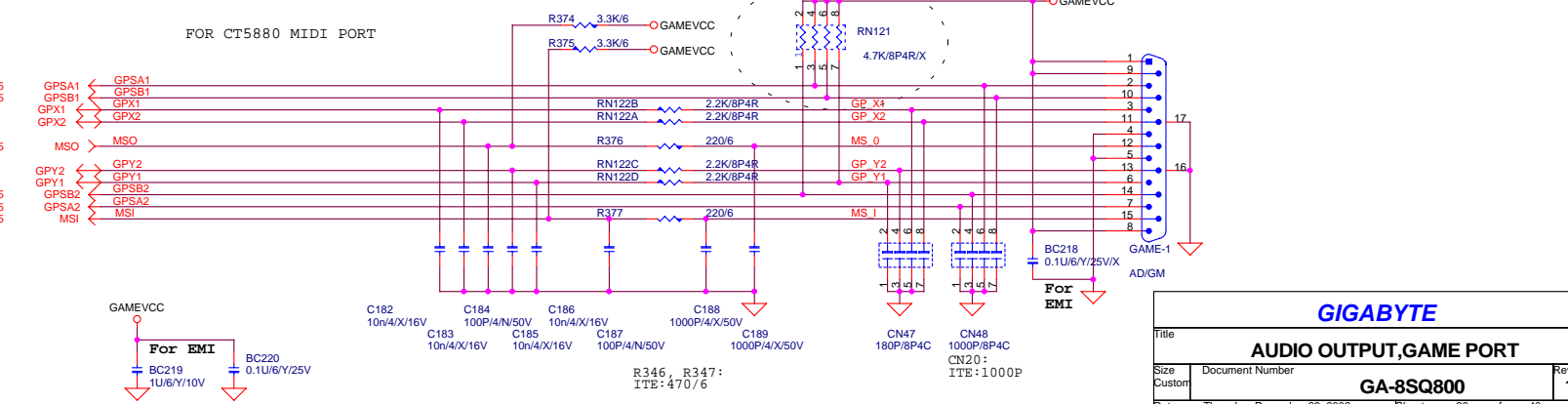
### AUX IN DEFAULT NO POP



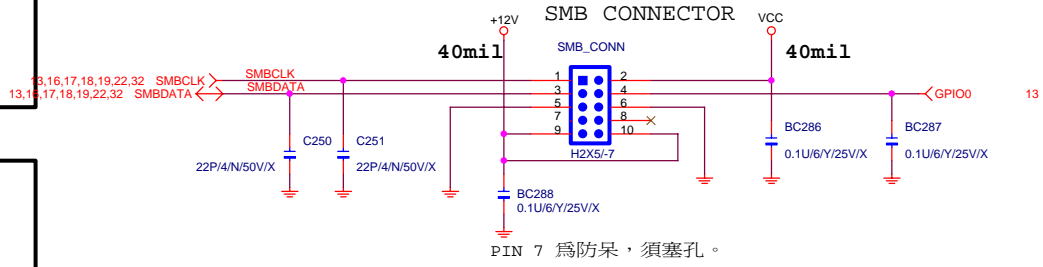
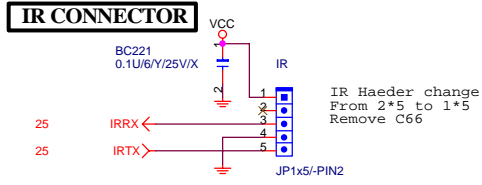
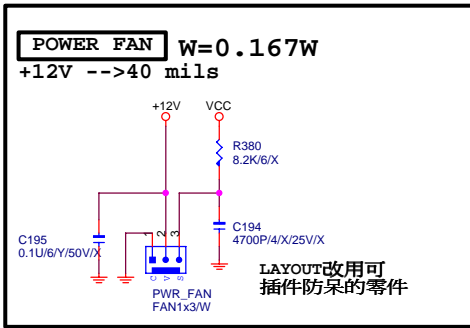
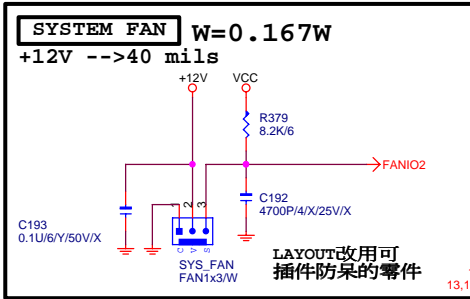
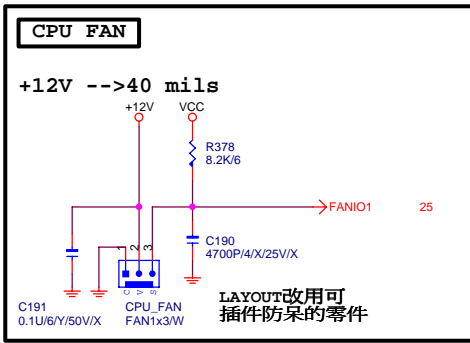
### CD IN



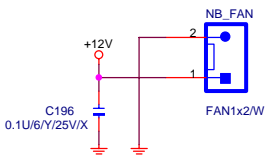
### GAME PORT



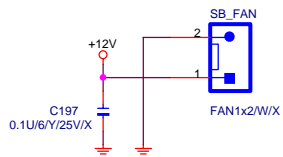
<b>GIGABYTE</b>	
<b>AUDIO OUTPUT, GAME PORT</b>	
Size	Document Number
Custom	<b>GA-8SQ800</b>
Date:	Rev <b>1.0</b>
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### NB HEAT SINK FAN

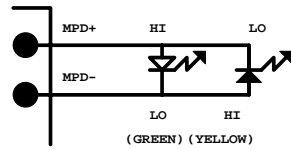


### SB HEAT SINK FAN



<b>GIGABYTE</b>		
<b>FAN</b>		
Size Custom	Document Number <b>GA-8SQ800</b>	Rev <b>1.0</b>
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**FRONT PANEL**



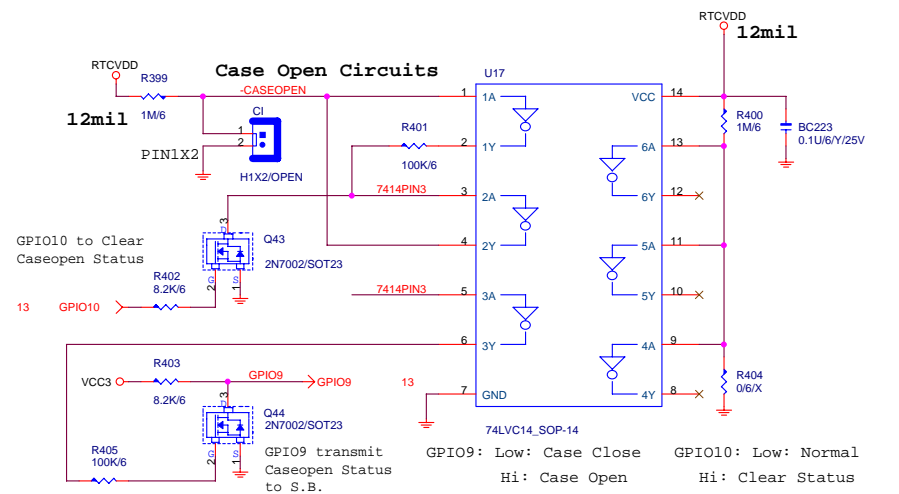
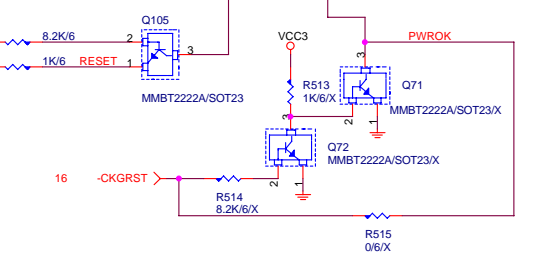
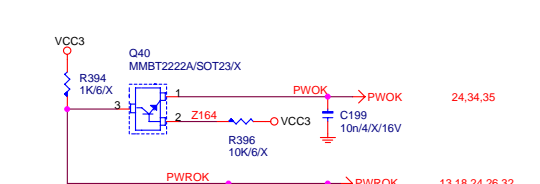
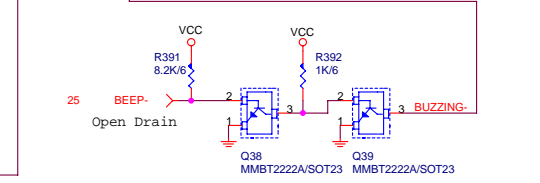
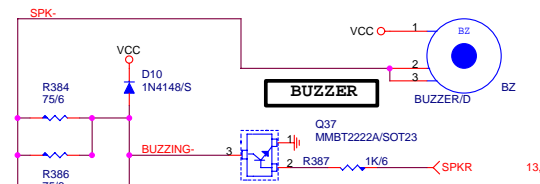
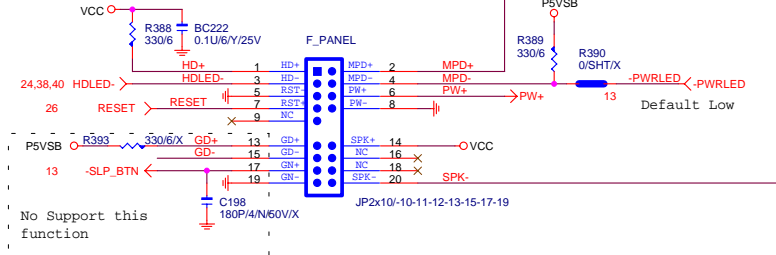
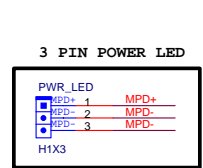
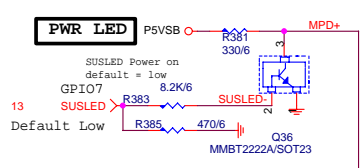
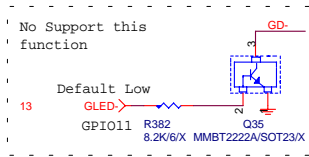
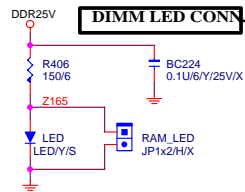
**States for a single-color power LED**

LED States	ACPI States	MPD+	MPD-
OFF	S1,S3,S5	HI	HI
Steady Green	S0	HI	LO
Blinking Green	S0(message waiting)	HI	BLINKING

**States for a dual-color power LED**

LED States	ACPI States	MPD+	MPD-
OFF	S5	HI	HI
Steady Green	S0	HI	LO
Blinking Green	S0(message waiting)	HI	BLINKING
Steady Yellow	S1,S3	LO	HI
Blinking Yellow	S1,S3(message waiting)	LO	BLINKING

	S0	S1	S3	S5
GPIO11 (GLED-)	0	1	1	0
GPIO7 (SUSLED)	0	B	B	0
ACPILED (Pin A15)	0	0	0	1



74LVC14:

10TC1-140014-01
10TC1-120014-01
10TC1-120014-02

GPIO9: Low: Case Close Hi: Case Open  
GPIO10: Low: Normal Hi: Clear Status

**GIGABYTE**

Title: **PANEL, STR LED**

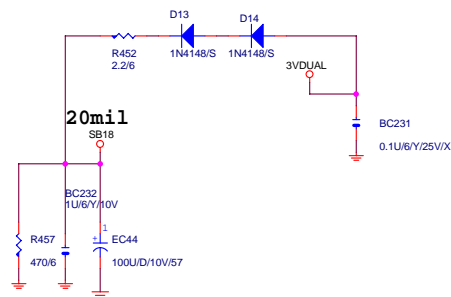
Size: Custom Document Number: **GA-8SQ800** Rev: **1.0**

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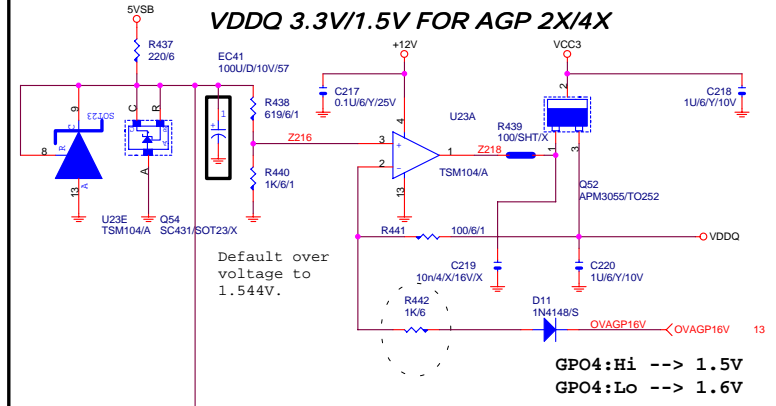




### SB18 FOR SB

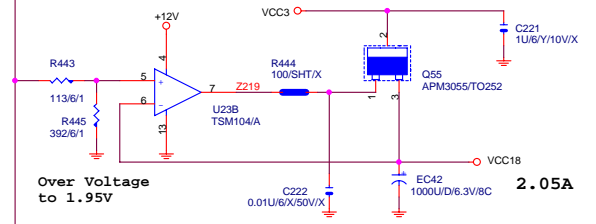


### VDDQ 3.3V/1.5V FOR AGP 2X/4X

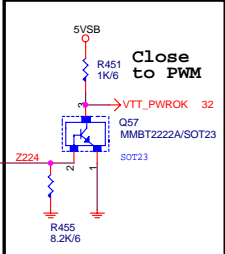
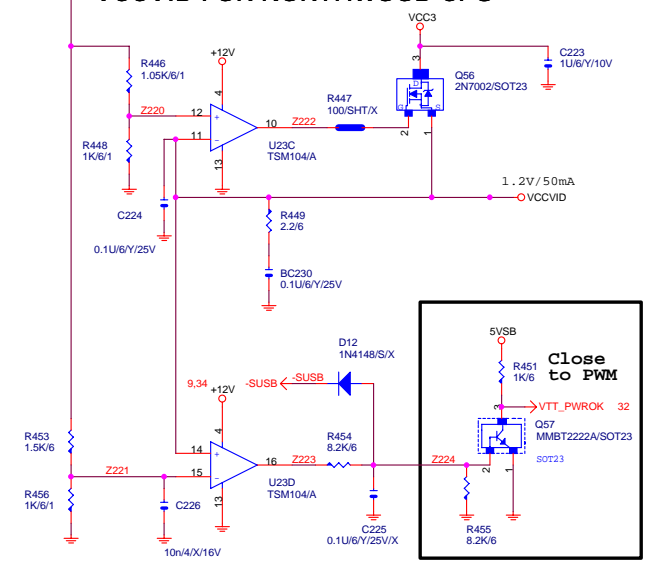


### VCC18 FOR NB,SB

Q55銅箔越大越好，盡量向右靠。

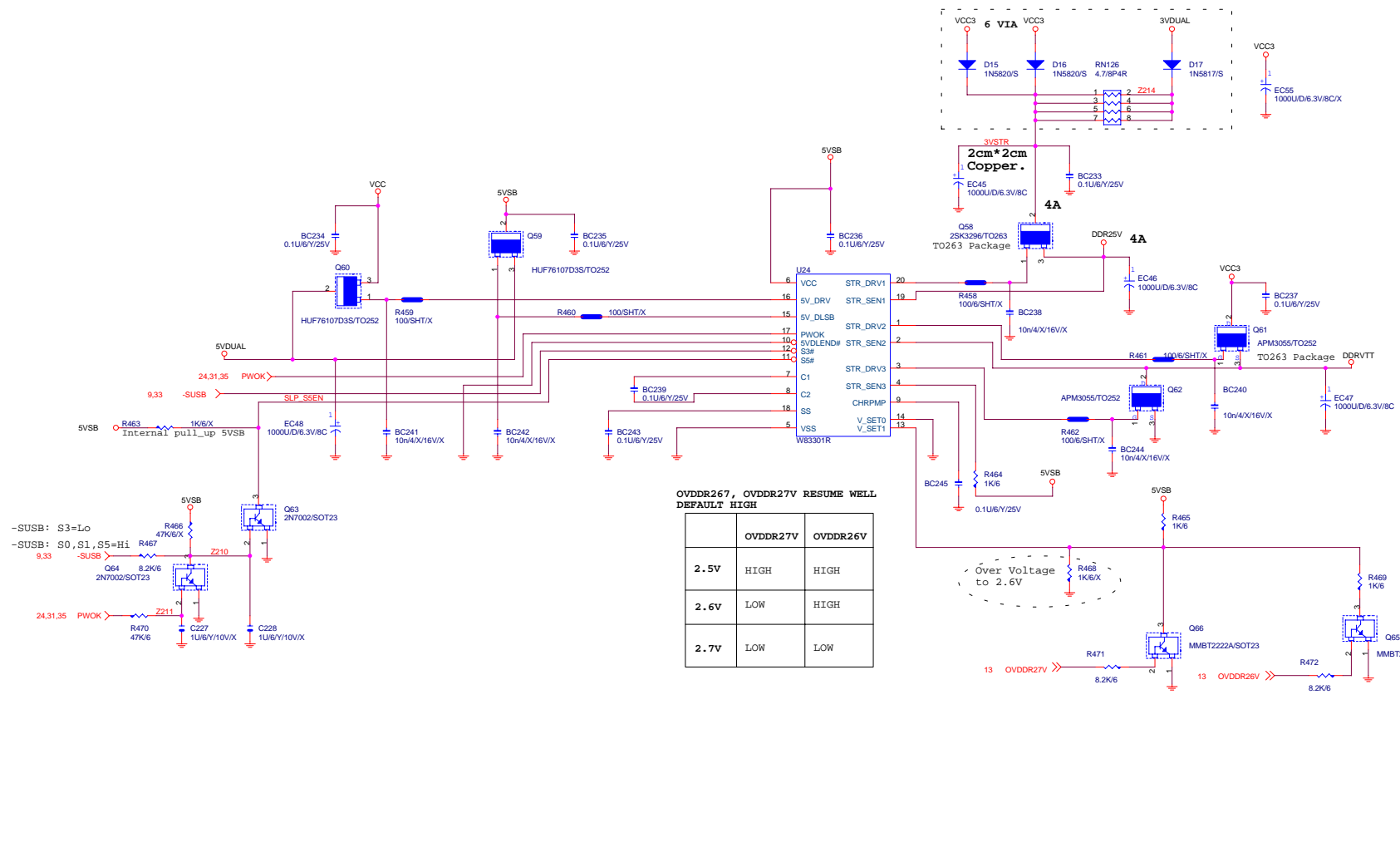


### VCCVID FOR NORTHWOOD CPU



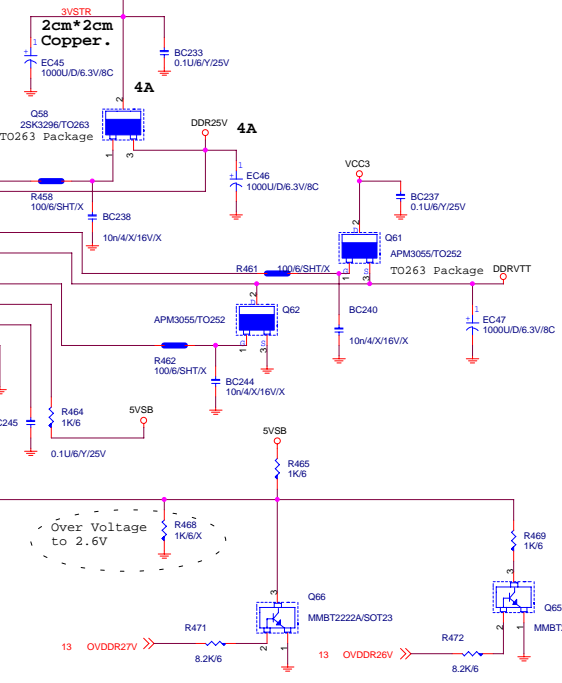
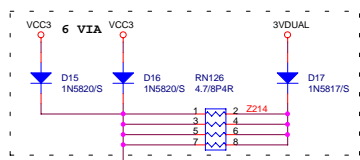
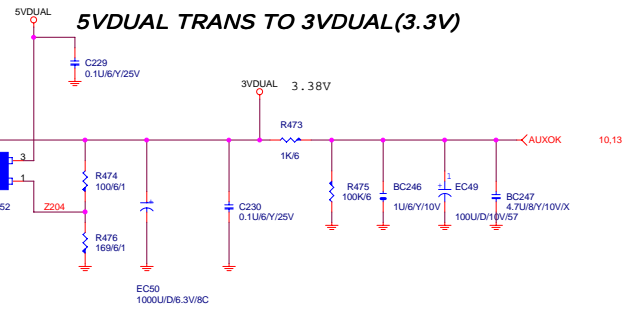
**GIGABYTE**

Title			VDDQ, VCCVID, 3VDUAL		
Size			Document Number		
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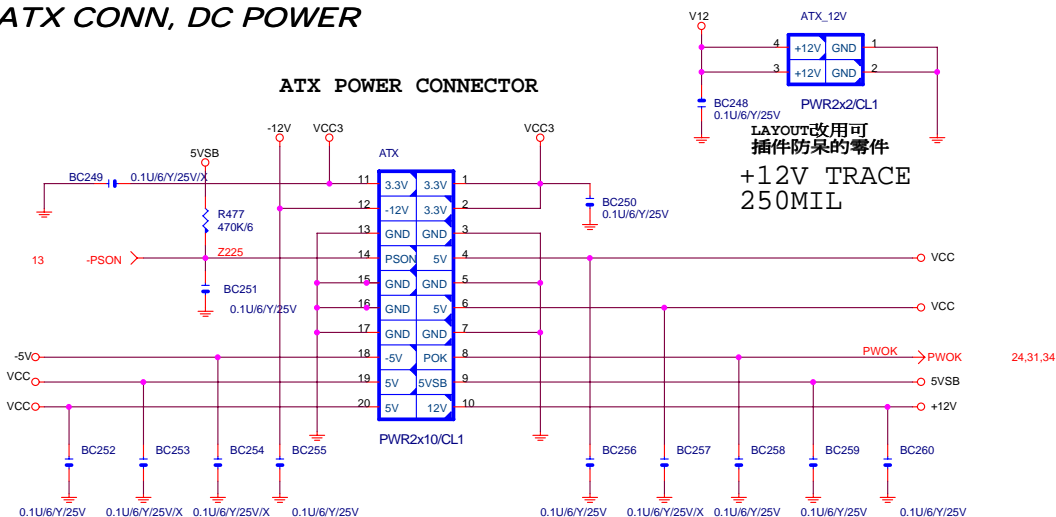
**OVDDR267, OVDDR27V RESUME WELL DEFAULT HIGH**

	OVDDR27V	OVDDR26V
2.5V	HIGH	HIGH
2.6V	LOW	HIGH
2.7V	LOW	LOW



# ATX CONN, DC POWER

## ATX POWER CONNECTOR



8SQ800 South Bridge GPIO LIST			
ITEM	DESCRIPTION	STATUS	Default
GPIO0	Non Use		Hi
GPIO1	Non Use		Hi
GPIO4	Non Use		Hi
GPIO2	Non Use		Hi
GPIO3	Green Button	Hi:Normal, Lo:Into Green mode	Hi
GPIO5	REQ5		
GPIO6	GNT5		
GPIO7	Non Use		Hi
GPIO11	Non Use		Hi
GPIO8	Wake On Ring	Hi:Normal, Lo:Ring Power On	Hi
GPIO9	Case Open	Hi:Case Open, Lo:Normal	Lo
GPIO10	Clear Caseopen status	Hi:Clear Caseopen Status, Lo:Normal	Lo
GPIO13	Non Use		Hi
GPIO12	Non Use		Hi
GPIO14	Primary Down	Lo:CODEC Only	Lo
GPIO15	KB Data		Hi
GPIO16	KB Clk		Hi
GPIO17	MS Data		Hi
GPIO18	MS Clk		Hi

### States for a single-color power LED

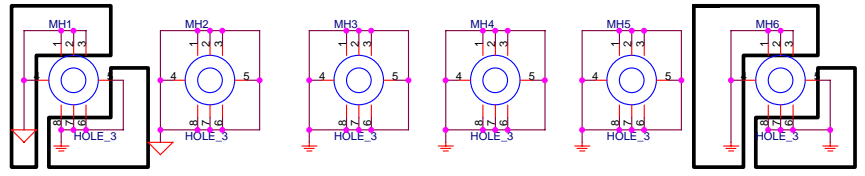
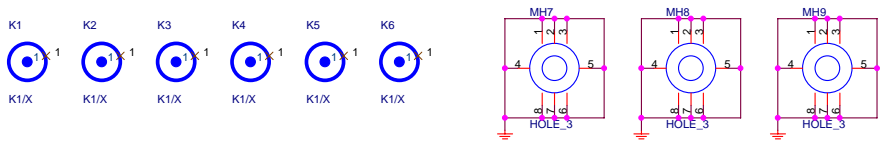
LED States	ACPI States	BIOS			
		MPD+	MPD-	GPIO7	ACPILED
OFF	S5	HI	HI	LO	HI/NC
Steady Green	S0	HI	LO	LO	LO
Blinking Green	S0(message waiting)	HI	BLINKING	LO	BLINKING

### States for a dual-color power LED

LED States	ACPI States	BIOS			
		MPD+	MPD-	GPIO7	ACPILED
OFF	S5	HI	HI	LO	HI/NC
Steady Green	S0	HI	LO	LO	LO
Blinking Green	S0(message waiting)	HI	BLINKING	LO	BLINKING
Steady Yellow	S1,S3	LO	HI	HI	HI
Blinking Yellow	S1,S3(message waiting)	LO	BLINKING	HI	BLINKING

### States for green LED

LED States	ACPI States	BIOS	
		GLE+	GPIO11
ON	S1,S3	HI	HI
OFF	S0,S5	LO	LO



EMI (VCC.GND CUT HOLE PLANE)

EMI (VCC.LGND CUT HOLE PLANE)

### BIOS REQUEST

SINGLE	DUAL	INTEL LED DEFINED				GIGABYTE LED DEFINED				SINGLE	DUAL
		GPIO7	ACPILED	GPIO11	GPIO11	GPIO7	ACPILED	GPIO11	GPIO11		
GREEN	GREEN	S0	LO	LO	LO	S0	LO	LO	LO	GREEN	GREEN
OFF	YELLOW	S1	HI	HI	HI	S1	LO	BLINKING	HI	G(BLINK)	G(BLINK)
OFF	YELLOW	S3	HI	HI	HI	S3	HI	HI	HI	OFF	YELLOW
OFF	OFF	S4/S5	LO	HI/NC	LO	S4/S5	LO	HI/NC	LO	OFF	OFF

**GIGABYTE**

**ATX, GPIO LIST**

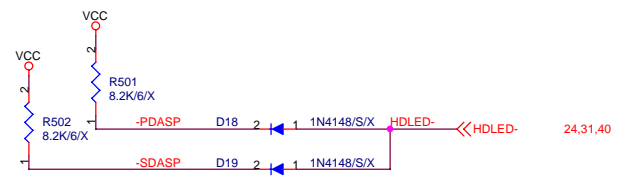
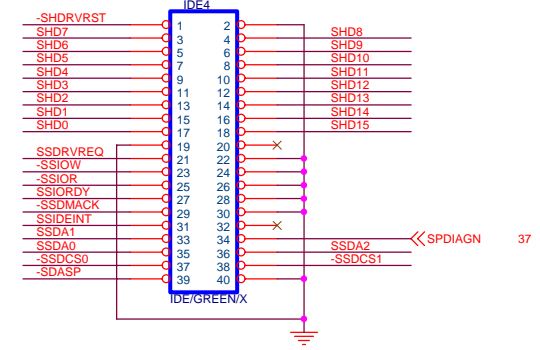
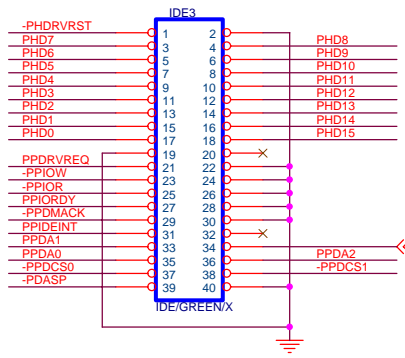
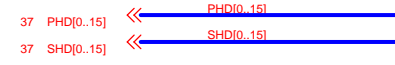
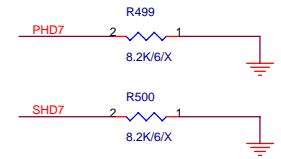
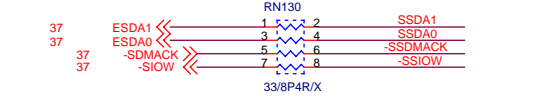
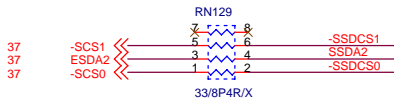
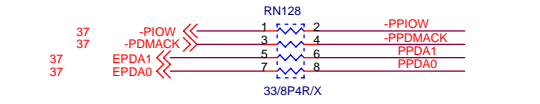
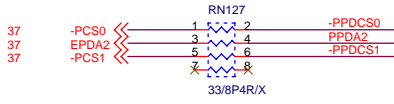
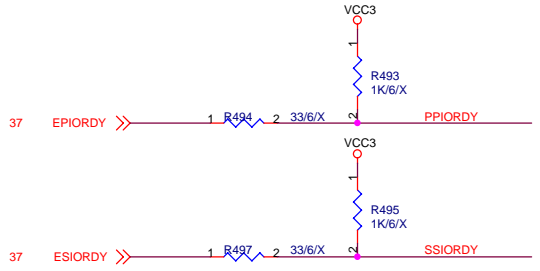
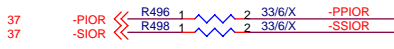
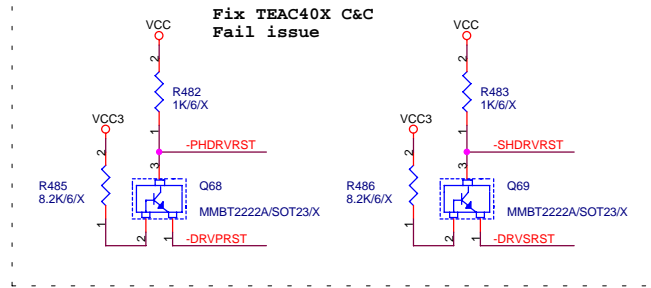
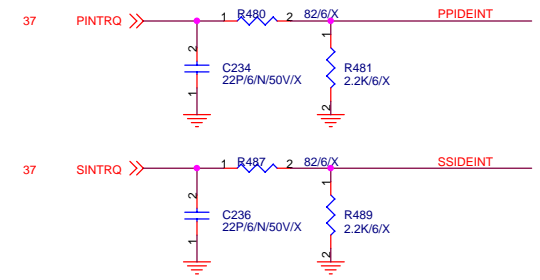
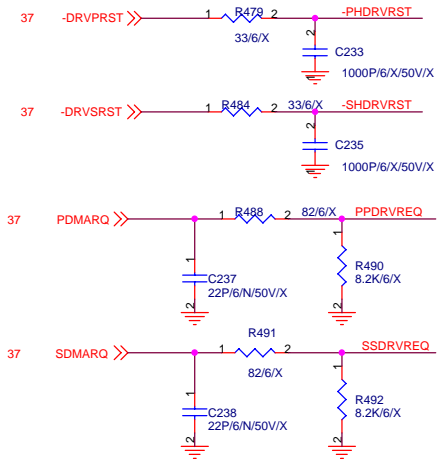
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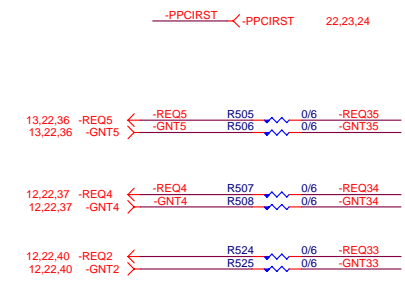
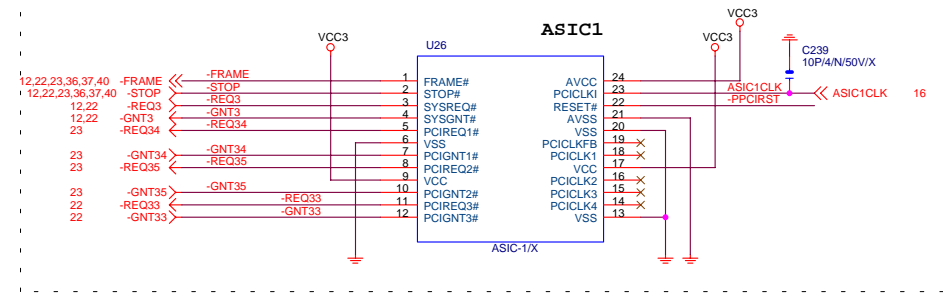
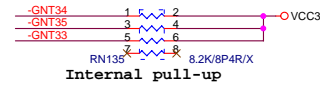
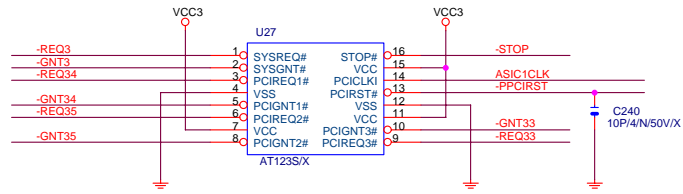
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	INTA#	IDSEL	REQx-
PCI1	BCDA	AD20	REQ0
PCI2	CDAB	AD21	REQ1
PCI3	DABC	AD22	REQ33
PCI4	ABCD	AD23	REQ34
PCI5	BCDA	AD24	REQ35
RAID	C	AD25	REQ4
RTL8101L	DB	AD26	REQ5
S-ATA	B	AD27	REQ2

**GIGABYTE**

**ASIC-1 & PCI ARBITOR**

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